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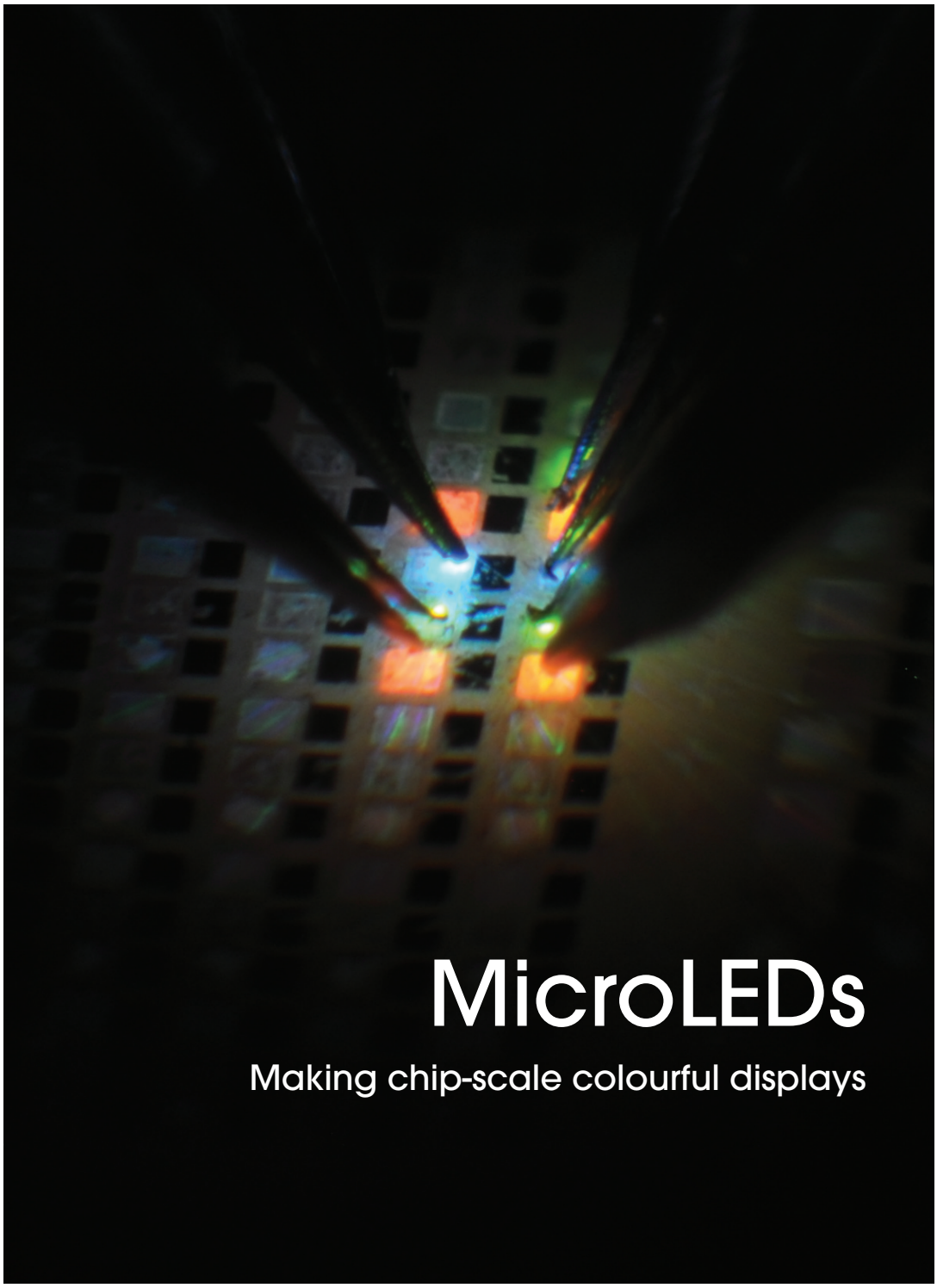

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Viewpoint

By Dr Richard Stevenson, Editor

Sweeping changes

WE ALL LIKE THINK that we can change direction when the need arises. But, in practice, it's not always easy. If we have spent years honing a particular skill, we will place great value upon it, and it is hard to walk away and embark on something new.

Based on this line of thinking, it is far easier for a new CEO to take a company in an entirely new direction than one that has invested much time and effort in developing what has been its core technology. And that's certainly the case for Cree. For several decades, it has been at the forefront of LED development, setting the pace with its unique technology: GaN on SiC. But margins in this sector are continuing to fall, the performance of those in the chasing pack is getting better and better, and it's a struggle to succeed. However, given all of Cree's investment in LED development, it would still be hard for a long-standing leader to switch the company's focus. But it's far easier for a newcomer – as Greg Lowe, the relatively new CEO is showing.

Since his arrival in the autumn 2017, Lowe has carved off the lighting business, redirected the company towards power and RF products – a move aided by the acquisition of Infineon Technologies' RF Power business – and decreed that the company will invest $1 billion in SiC. LEDs are still being made, but their foundation is shifting to sapphire, to free up SiC capacity.

We recently caught up with Lowe, discussing the details of the company's investment, which will grow capacity by a factor of 30 (see p. 14 for details). To realise this, two existing wafer

fabs will be reconfigured into what are described as materials mega factories, and a 200 mm power and RF wafer fabrication facility will be formed in an existing facility. By the mid 2020s, production will be shifting from 150 mm to 200 mm wafers to coincide with a ramp in demand for electric vehicles. To support the latter, the company is already forming strong partnerships. For example, it has just been selected by the Volkswagen Group to join the 'Future Automotive Supply Tracks' initiative.

Right now, Cree is going through a turbulent time, due to a softening of the LED market, and legislation preventing the company from shipping its products to Huawei. But I'm sure that in the long-term we will see revenues rocket, and the company positioned at the forefront of a power electronics revolution.

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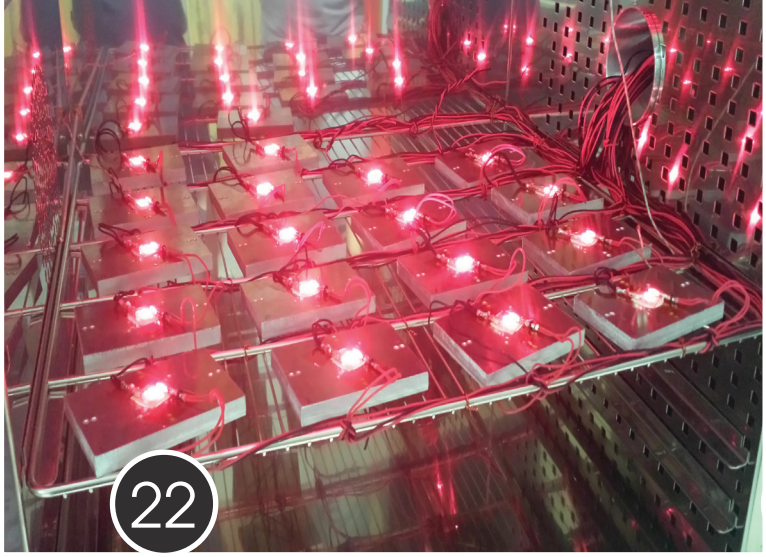

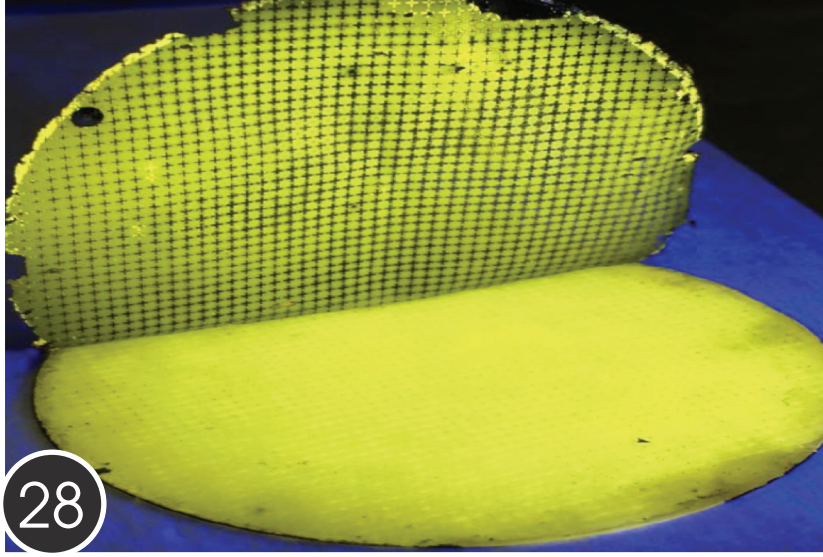

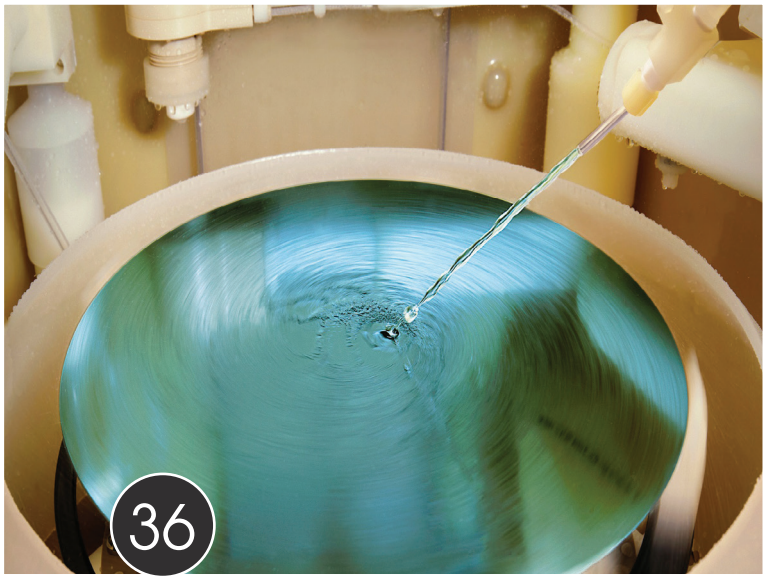

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Riber licenses innovative *in-situ* control tech from LAAS-CNRS

RIBER has signed an operational licensing agreement with Toulouse Tech Transfer (TTT), a regional operator for creating value and transferring technology from public research, for the exclusive marketing of a reflective surface defect and curvature measurement technology, developed by the Laboratory for Analysis and Architecture of Systems (LAAS-CNRS), one of the French National Centre for Scientific Research's largest in-house units.

Today, several techniques enable the monitoring of deposition deformations in real time and with a non-invasive approach. However, these systems are not very precise, are generally complex to implement, expensive and can only be used in certain specific experimental conditions.

The LAAS-CNRS researchers Alexandre Arnoult, research engineer, and Jonathan Colin, post-doctoral researcher, have developed a sophisticated optical device that is said to be easy to implement and helps to significantly improve control over operations to deposit thin films. The device can be used in any type of environment.

This makes it possible to measure curvature and defects on all types of surfaces in real time and over significant production times. For example, it helps to avoid dislocations, produce perfectly even wafers or control deposit consistency. The device will also be equipped with machine learning algorithms that will be specially developed to optimise analysis and control for the materials growth process. The know-how based on this research, marketed under the new EZ-Curve brand will enable Riber to extend its range of solutions and services, providing research laboratories and semiconductor manufacturers with added value in line with their needs.

For industrial users, ensuring the traceability and reliability of their measurements is key to effectively manage their manufacturing processes and guarantee product quality and performance. For researchers, analysing and understanding materials growth-related behaviors makes it possible to expand fundamental knowledge. The EZ-Curve solution is said to be a major MBE innovation. In addition to controlling the epitaxial growth process with high-precision 3D reflectance metrics, this device also offers wider possibilities by supporting the implementation of automated advanced control processes and, over the longer term, the development of smart MBE systems, according to Riber.

Philippe Ley, Riber's CEO said: "EZ-Curve is a significant technological innovation compared with the measurement instruments currently available on the market. Our ambition is to provide our clients with the very precise levers needed to considerably improve their processes and the results of their developments, whether they are academic or industrial. This new technological component and its industrialisation will make it possible to further strengthen MBE performance capabilities".

"Monitoring a wafer's deformations during the vacuum growth or processing of a thin film represents an unrivalled source of information on the atomistic processes involved, and quality control for industrial processes. Until now, this monitoring was reserved for specialists using tools that were complex to master. Our new technology successfully makes it possible to achieve this combination of increased sensitivity with outstanding robustness and simple implementation, which enables to deploy it across a large number of advanced and/or production systems. For example, we can now continuously monitor molecular beam epitaxy growth for complex semiconductor structures with low constraints, opening up possibilities for *in-situ* feedback control during processes, and therefore optimization and automation of processes", confirms Alexandre Arnoult, LAAS-CNRS.

Following maturation and market release phases, Riber, the LAAS-CNRS and TTT intend to continue sharing their knowledge in order to support this product's development worldwide. The technology transfer by TTT's teams has focused on creating value and industrialising the EZ-Curve solution in order to facilitate its integration and its marketing by Riber. This 100th license set up by TTT is a major milestone in its development since it was created in 2012. It illustrates the numerous actions carried out to create value through and capitalize on French public research to support national competitiveness.

Pierre Dufresne, CEO of Toulouse Tech Transfer, is delighted with this 100th license: "This is the result of the collaboration between teams from Riber, the LAAS-CNRS and TTT. They have worked on this transfer with enthusiasm and pragmatism. Throughout the project, the teams have remained available and successfully worked with confidence to achieve their goals. TTT is proud to have been able to contribute to this technology's maturation so that Riber can rapidly bring its innovative product to the market".

IQE share price nosedives on trading update

SHARES in IQE, a leading global supplier of advanced wafer products and materials to the semiconductor industry, fell by about one-third after the company provided a trading update ahead of the financial close for the first fiscal half of 2019.

The Cardiff-headquartered firm now expects to deliver revenue of £65 million to £68 million for the first fiscal half of 2019, a range at the bottom end of previous guidance. Of more concern is the revised forecast for the second fiscal half of this year. IQE now expects to generate sales of £140 million to £160 million, below the previous expectation of £175 million. The company still expects to remain profitable in 2019. However, its Adjusted Operating Profit margin will be significantly below the previous guidance of over 10 percent.

IQE's revised figures reveal that trading conditions are having a larger impact than the previously guided risk related specifically to Huawei. This is due to the far-reaching impacts on other companies and supply chains that are now becoming evident.

The photonics segment is now expected to grow by less than 30 percent year-on-year, rather than 50 percent, the figure given in previous guidance.

Headwind for IQE has come from geo-political uncertainties. The company says that it may experience some delay to orders and the potential for adjustment of supplier managed inventory levels, predominantly in its wireless business unit.

The company believes that it is now operating in an increasingly cautious marketplace. It has very recently received a reduction in forecasts from a number of chip customers, in wireless and also in photonics divisions. These changes impact anticipated revenues for the second fiscal half of this year.

The trading update follows an earlier announcement this year, when IQE stated the sales for the first half of fiscal 2019 has been impacted by a weak smartphone handset market, particularly affecting its wireless business unit. In addition, it said that it had also experienced a reduction in InP laser revenues for the datacom market due to a customer specific issue outside of IQE's control. This has been partially offset by new qualifications and revenue streams coming into production at the company's Taiwan facility where it has invested in capacity and now offers increased customer diversification.

Another encouraging sign for IQE is a substantial order placed with the company's recently constructed Newport Mega Foundry. It is this site's first mass

production order, and it has come from IQE's leading existing VCSEL customer. This has had a beneficial impact on photonics revenues for May and June, in line with previous guidance.

At Newport Mega Foundry for VCSEL production, four reactors are currently in mass production with the first major customer. Two further customers are expected to enter mass production in the second half of this year.

Sampling continues with an additional 13 customers as part of ongoing qualifications, which provides breadth of exposure to global supply chains. IQE remains confident that it will continue to show strong revenue growth in the photonics business through customer diversification in 2020 and beyond.

JBD develops 2.5 micron pitch micro-LED display

HONG KONG-BASED Jade Bird Display Ltd (JBD) has recently demonstrated what the company believes is a record-breaking 2.5 μ pixel pitch active matrix microLED display panel.

The 2.5 μm pitch display panels were fabricated by JBD's proprietary hybrid integration technologies. In a hybrid integration process, ultra-thin InGaN (for blue and green) and AlInGaP (for red) epitaxial layers were first grown on their substrates, such as sapphire and GaAs, by MOCVD.

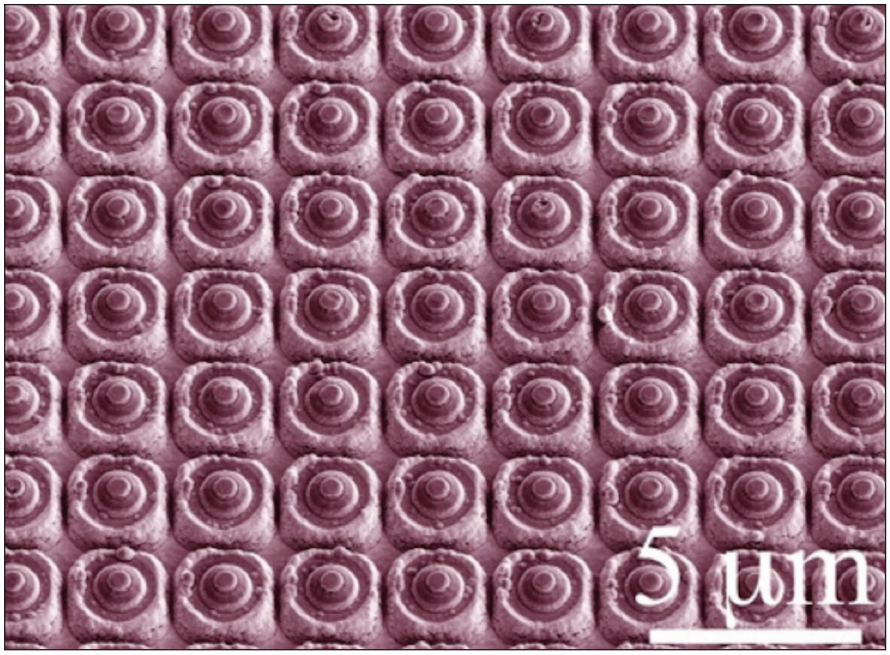
The complete sheets of epitaxial layers were then separated from the substrate wafers and bonded to CMOS wafers at a temperature below 350°C. Such wafer-level epi transfer eliminates the need of alignment bonding and dramatically increase the pixel yield, uniformity, and manufacture throughput.

Following the epilayer transfer, standard lithography and etch steps were performed to transform the thin sheets of epilayers into emitter arrays on the CMOS backplane wafers. Electrical contacts were subsequently made by cycles of lithography, passivation, and metallisation.

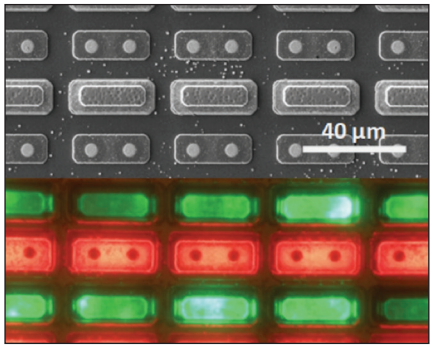
Before the wafers were diced into chips, optical elements, such as micro-lens and reflector arrays were finally fabricated on the emitters in a monolithic wafer-level scale. To achieve desired light collimation, the emitter mesa diameters were designed to be approximately a third of the pixel pitch. Therefore, for the 2.5 μm pixel pitch, the emitter mesa diameter is less than a micrometer, as shown by the scanning electron microscopic image in Fig. at the top of the page.

As well as pushing the boundaries of monochromatic pixel emitter dimensions, the company is also exploring polychromatic micro-display panels.

These polychromatic panels were fabricated by stacking multiple sheets of blank epilayers on a CMOS backplane wafer. The epilayer stacking was then followed by III-V/ compound semiconductor thin film processing sequences. Without using alignment bonding or pick-n-place, desirable pixel yield and uniformity can be achieved.



AMuLED display panels fabricated by JBD's proprietary hybrid integration technologies



A scanning electron microscopy image of a proof-of-concept bicolour pixel array with a pitch of 40 μm (above) and optical microscopy image (below) of lit pixels in a wafer level test.

As compared to DLP and LCOS, the display panels do not require illumination light sources. Light emission from III-V/ Nitride compound semiconductors and digital image control from CMOS were integrated in a 0.5 mm thick chip. This hybrid integration significantly reduces the complicity of the optics in VR or AR devices.

Moreover, the compound semiconductor emitters deliver much higher light output intensity compared with OLED micro emitters.

For example, JBD's 2.5 μm pixel pitch display panels offer 1 million cd.m^{-2} at 525 nm, which is several orders of magnitude higher than that reported for OLED micro-display performance. Furthermore, without any moving parts and containing no organic materials, the display panels can be used in wide temperature ranges (-50°C to 100°C) and harsh environment (vibration and UV radiation) with high reliability and long life time.

Founded in 2015, JBD is currently transitioning from a research-and-development phase into a manufacturing-and-sales phase. In April 2019, JBD released a 5μm-pitch series.

This series contains monochromatic panels with a resolution of 1280 by 720. The 2.5 μm pitch series is scheduled to be released in late 2020. With a pilot fab established in Shanghai China, JBD continues to expand its manufacturing capacity and extend its development effort to support its customers.

Northrop Grumman's $958 million GaN radar contract

THE US MARINE CORPS has awarded Northrop Grumman a $958 million contract for Lot 6 full-rate production of the GaN-based AN/TPS-80 Ground/Air Task-Oriented Radar (G/ATOR) systems. This contract provides an additional 30 units.

"Northrop Grumman and the Marine Corps have successfully partnered to create a best of ground and airborne radar solution that exceeds the current threat on the modern battlefield," said Christine Harbison, vice president, land and avionics C4ISR, Northrop Grumman.

"G/ATOR is a crucial capability that protects our warfighters and defends against today's threat environment and the threat environment of the future. We are excited to reach the full-rate production decision and continue providing advanced multi-mission functionality that meets our customer's mission needs, protects the warfighter in a rapidly changing threat environment, and has significant margin for capability growth."

G/ATOR replaces five legacy systems operated by the Marine Corps with a single system, providing significant improvements in performance when compared with the legacy radar families in each of its modes. This results in reduced training, logistics and maintenance costs.

The AN/TPS-80 G/ATOR is an advanced Active Electronically Scanned Array (AESA) multi-mission radar that leverages GaN to provide comprehensive real time, full-sector, 360° situational awareness against a broad array of threats. The highly expeditionary, three-dimensional, short-to-medium-range multi-role radar system is designed to detect, identify, and track cruise missiles, manned aircraft and unmanned aerial vehicles as well as rockets, mortars and artillery fire.

Sofradir and ULIS become Lynred

INFRARED specialist Sofradir, based in Grenoble, France and its subsidiary ULIS have announced their merger and a new company name: Lynred.

Lynred was created to respond to a need for an all-inclusive infrared (IR) product offering to the global aerospace, defence, industrial and consumer markets. In response to increasing market requirements, the company has attained a critical mass geared to shortening the time-to-market process of new products. Its US entity remains a subsidiary and has been renamed Lynred USA.

Lynred is the new identity under which its 1,000 staff will provide the widest range of advanced IR technologies to global markets, assure a long-term and reliable product supply and accompany client projects with the best possible IR design and equipment integration support. "Lynred will enter the market with a new vision for the future in an increasingly competitive market, which has seen the number of players double over the last five years," said Jean-François Delepau, chairman of Lynred. "We are the established European leader in infrared technologies. Now, Lynred gives us more punching weight in R&D and increased visibility within the IR ecosystem. Thanks to the commitment of our employees in forming Lynred and increased support from our partners, we will be able to offer new attractive solutions to our customers." Lynred is actively pursuing growth in this market. The world military infrared imaging systems market was estimated at $8.5 billion (approx. €7.6 billion) in 2018 and is expected to grow to $14 billion (approx. €12.5 billion) in 2023. Extrapolated market data also indicates that the market for cameras for industrial and consumer applications has the potential to increase from $2.9 billion (approx. €2.6 billion) to $4.1 billion (€3.7 billion) in the same period. This translates to a global potential annual market growth rate of around 10 percent at camera and system level.

Lynred will advance developments of next generation IR detectors with the €150 million ($167.4 million) financial investment it is making in the Nano2022 project over the next five years. These IR devices will be designed to address trends in autonomous systems for smart buildings (workspace management, energy savings), road safety and in-cabin comfort of vehicles. Developments also include the very large dimension IR detectors needed for space and astronomy observations as well as compact and light IR detectors that can be used in portable devices and on drones. Lynred will continue enlarging its product catalogue, strengthening its R&D investments and hiring in support of activities.

EPC and Spirit partner on GaN data packs

EPC has announced a partnership with Spirit Electronics to provide an expanded range of manufacturing lot-specific data services for their enhancement-mode GaN devices.

"Our partnership with Spirit Electronics provides the opportunity for EPC to complement Spirit's extensive history and proven successful track record in working with defense and aerospace customers," commented Alex Lidow, CEO and co-founder of EPC. "Offering lot-specific data services related to our eGaN power semiconductor products will enable us to bring additional value to these demanding applications."

Marti McCurdy, CEO of Spirit Electronics, noted that, "Our partnership with EPC has been an exciting addition to our portfolio of products and this new offering of lot-specific data services will further help us bring the superior performance of eGaN power transistors and ICs to defence and aerospace customers, so they can design leading-edge power system solutions."

Integra wins US Air Force contract

INTEGRA TECHNOLOGIES has been awarded a two-year contract by the US Air Force to accelerate technology and manufacturing readiness of its patented, thermally-enhanced GaN/SiC technology. Integra's GaN/SiC technology is designed for high efficiency, solid-state RF power applications including high power radar systems requiring improved performance, increased range and reduced operating costs.

The company has developed its thermally enhanced GaN/SiC to deliver superior power and efficiency while operating at lower temperatures which is a key enabler of next generation high performance radar platforms.

The company is using its domestic R&D and manufacturing platform to optimise the GaN epitaxial wafer, device design and package design. Additionally, the US Air Force contract will enable robust qualification of Integra's thermally enhanced GaN/SiC for production.

"We are excited to work with the Air Force," said Suja Ramnath, president and CEO of Integra Technologies. "Through this effort, we have the opportunity to commercialise our leap-ahead GaN/SiC technology to meet the high efficiency performance and production readiness requirements of the US Department of Defence."

II-VI introduces high power collimated laser bars

II-VI, a maker of high power semiconductor lasers, has announced the introduction of its high power laser bars and semi-framed stacks mounted with micro-optic collimator lenses, offering customers cost-effective modular assemblies that have high performance and reliability and can be easily integrated into direct diode lasers and diode-pumped solid state (DPSS) lasers.

Direct diode and DPSS lasers are increasingly the tools of choice for a wide range of materials processing, biomedical, and defence applications, due to their compact form factor, high power short-pulsed operation, and availability over a broad range of wavelengths from near-infrared to ultraviolet. The performance, quality, reliability, and cost of these systems are highly dependent on those of their semiconductor laser sub-assemblies. II-VI says that it now combines its high power laser bars and new simplified semi-framed stack structures with fully automated optical alignment processes to deliver modular assemblies at optimal cost.

"Our laser bars feature a proprietary hard solder technology that withstands high power pulsed operation with field-proven reliability," said Chris Koeppen, vice president of II-VI Industrial Laser Group. "We now efficiently deliver optimal custom designs by leveraging the automated assembly processes in our direct diode manufacturing lines. These processes enable a variety of micro-optics, such as collimator lenses and volume Bragg gratings, to be cost-effectively mounted and precisely aligned to a broad range of customer-defined stack geometries."

GaN and GaAs deliver RF for internet of satellites

QORVO has announced that its amplifiers are being used in the telemetry tracking and control modules developed by Syrlinks for Low Earth Orbit (LEO) satellites. The first six satellites of the constellation, designed by Airbus OneWeb Satellites, were recently launched to provide internet connectivity practically anywhere in the world. The industry-leading reliability and performance of the Qorvo products reduce stress on the satellite power systems and ensure signal integrity in both transmit and receive modes.

Close collaboration and flexibility across both companies' functional teams were key to the success of this project. Syrlinks integrated the Qorvo RF front-end components into the space-qualified module and provided product definition and performance requirements for the Qorvo products. Qorvo provided product application, manufacturing and test support. The MMIC power amplifier selected is built on Qorvo's 0.15 μm GaN process, QGaN15, which supports high-frequency applications through 40 GHz. The Low Noise Amplifier is built on Qorvo's 90 nm GaAs pHEMT process, QPHT09, which is said to have best-in-class noise figure. Qorvo has nearly 100 commercial products (die and package options) built on these processes.

Guy Richard, Syrlinks' CEO, said: "Syrlinks has been investing for three years in the NewSpace approach associated with the latest generation of components. These efforts required stronger links with manufacturers of high-performance and innovative components, such as Qorvo. We are always looking for the best in terms of performance and reliability."

Roger Hall, general manager, Qorvo High Performance Solutions, said: "Qorvo's commercially-packaged products are proving their operational readiness to meet the harsh environment of space. By combining powerful process technology with advances in packaging, Qorvo is enabling high power devices that also achieve high reliability and are operationally rugged."

Syrlinks specialises in radio communication and geolocation subsystems for space, defense and safety applications. Its NewSpace products perfectly meet the new requirements of the space industry. Syrlinks' telemetry, tracking and control modules enable remote sensing and monitoring of the Airbus OneWeb LEO satellites for internet connectivity service.

Macom wideband amp covers 30 kHz to 40 GHz

MACOM has announced a new wideband distributed amplifier for test and measurement applications.

The MAAM-011275-DIE, which is offered as a bare-die device, is designed for use in test and measurement (T&M) and communications equipment with broadband frequency coverage from sub-6 GHz to mmW. The amplifier supports operation from 30 kHz up to 40 GHz with typical gain of 15 dB. The input and output are fully matched at 50 Ω with typical return loss of 13 dB across the band.

NXP sets RF energy efficiency benchmark with GaN transistor

AT THE International Microwave Symposium 2019 in Boston NXP Semiconductors announced the first RF power transistor designed for RF energy using GaN-on-SiC. Using the high efficiency of GaN, the MRF24G300HS exceeds the efficiency of most magnetrons at 2.45 GHz, while the high thermal conductivity of SiC helps to ensure Continuous Wave (CW) operations.

For more than 50 years, 2.45 GHz magnetrons have been widely used in consumer and industrial applications ranging from microwave ovens to high power welding machines. Solid-state solutions appeared on the market several years ago, bringing advanced control, reliability, and ease of use. The capability to dynamically adjust the power, frequency, and phase helps optimise the energy transmitted to the material or food being heated. The long lifetime of transistors at full rated performance reduces the need for replacements. However, until the advent of GaN-on-SiC for RF Energy, solid-state devices lacked efficiency to meet the performance standards of the incumbent magnetrons.

The MRF24G300HS is a 330 W CW, 50 V GaN-on-SiC transistor, demonstrating 73 percent drain efficiency at 2.45 GHz, which is five points higher than the latest LDMOS technologies. The high power density of GaN enables the device to reach high output power in a small footprint. GaN technology has an inherently high output impedance that allows broadband matching compared to LDMOS. This reduces the design time and ensures consistency on the manufacturing line as no more hand tuning needed. The simplified gate biasing of the MRF24G300HS RF transistor removes another step of the otherwise complex power-up sequence typically seen on GaN devices. NXP's MRF24G300HS RF transistor is sampling now and production is planned for Q3 2019. The 2400-2500 MHz reference circuit is available now, under order number MRF24G300HS-2450MHZ. As part of the NXP Partner Program, Prescient Wireless, designed a 2-up, 550 W power amplifier pallet with 45 dB of gain, that was shown at IMS.

Wentai uses Transphorm power supply

TRANSPHORM, a maker of hi-rel JEDEC- and AEC-Q101 qualified high-voltage (HV) GaN semiconductors, has confirmed that Taiwanese OEM Wentai Technology has developed a Titanium ATX gaming power supply series called Aidan that uses Transphorm's TP65H050WS Gen III 50 mΩ GaN FET in an interleaved CCM boost PFC.

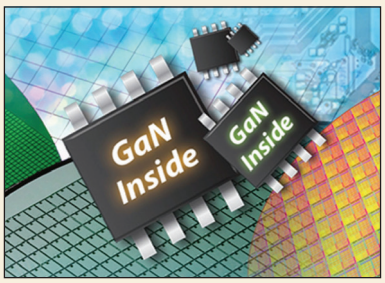
The result is a fully-modular, low-noise 1.6 kW 80 PLUS Titanium power supply unit (PSU) with close to 95 percent efficiency. The Aidan ATX PSU series targets consumer computing markets requiring ultra-high power such as PC gaming, Esports, artificial intelligence (AI), and cryptocurrency mining. When compared to Wentai's silicon-based 1.28 kW PSU, the Aidan-T1616 offers 328 W more power and approximately one percent higher efficiency at 50 percent full load – all within the same form factor. This equates to a 20 percent increase in power density. "The high-performant PC market serves use cases such as immersive gaming, artificial intelligence (AI) and virtual currency mining that requires a large amount of reliable power in comparison to everyday PC use," said Aidan Liao, senior R&D director, Wentai.

Wentai's power system development project occurred over the course of 18 months. Throughout that time, the company worked with Transphorm's regional application support team whose positive reputation, according to Liao, was another influencing factor behind Wentai choosing Transphorm's GaN devices.

EPC to provide eGaN devices in wafer form

EPC announces the availability of its enhancement-mode GaN (eGaN) devices in wafer form for ease of integration. EPC's eGaN FETs and ICs are traditionally sold as singulated chip-scale devices with solder bars or solder bumps.

Chip-scale packaging is a more efficient form of packaging that reduces the resistance, inductance, size, thermal impedance, and cost of power transistors. These attributes of eGaN devices enable unmatched in-circuit performance at competitive prices.



Wafer-level offerings of these devices allows for easier integration in customer power system sub-assemblies, further reducing device interconnect inductances and the interstitial space needed on the printed circuit board (PCB). This increases both efficiency and power density while reducing assembly costs.

"We have listened to our partners and are pleased to offer our industry-leading GaN products in wafer form that can accommodate a variety of assembly techniques and applications," commented Alex Lidow, CEO and co-founder of EPC.

EPC is offering eGaN power devices in wafer form either with or without solder bumps. Extra services such as wafer thinning, metallisation of the wafer backside, and application of backside coating tape are also available.

CSC announces partnership £9.8 million SiC project

THE COMPOUND SEMICONDUCTOR CENTRE is a partner in a project which has been awarded £9.8 million in funding through the UK's Advanced Propulsion Centre (APC).

The ESCAPE project (End-to-end Supply Chain development for Automotive Power Electronics) will create a complete end-to-end supply chain for next generation SiC Power Electronics, which is a key component to be used in all electric vehicles, whether automotive, railway, marine or aviation - a first for the UK.

This funding is part of the UK government's £33 million investment through APC to advance the UK's low-carbon automotive capability and to develop the next generation of low-carbon vehicles, helping the automotive sector build a prosperous low-carbon future. The ESCAPE project, let by McLaren Applied Technologies, is one of five projects awarded funding, ranging from the development of high-performance battery packs and electrified construction equipment, to hydrogen powered engines.

Twelve other partners will support the creation of the integrated supply chain, including other industry leaders such as AESIN, Clas-Sic Wafer Fab, the Compound Semiconductor Applications Catapult, Exawatt, Lyra Electronics, MaxPower Semiconductor, Tribus-D, Turbo Power Systems and The University of Warwick.

Wyn Meredith, CSC director commented: "The demand for SiC power components is growing rapidly, and we welcome the opportunity to work with our partners to ensure the UK has a world class future supply chain in this critical technology ".

Lumileds targets surveillance with Luxeon IR range

LUMILEDS has announced the latest addition to its Luxeon IR family, the Luxeon IR Domed Asymmetric, that matches the Field-of-View (FoV) aspect ratio of typical cameras used in surveillance, machine vision and time-of-flight systems. The 95 x 58 inch design dramatically improves image uniformity.

The Luxeon IR Domed Asymmetric delivers radiant power of 1350 mW at 850 nm and 1450 mW at 940 nm. The emitters are offered in a 3.7 mm x 3.7 mm package with standard 3-pad configuration for direct upgrade of existing circuit board designs.

Component quality is ensured by the use of the highest quality silicone dome, gold-finished solder pads and gold-based bond wires for corrosion resistance. The ceramic package uses the industry's lowest thermal resistance substrate (2.5°C/W) for rapid removal of heat, smaller optics and more compact camera designs.

Cree: Full Speed Ahead?

Will Cree's bold plans for SiC expansion be thwarted by rising US-China tensions, asks Rebecca Pool

AS THE DUST SETTLES on the industry news that Cree is to invest a mighty $1 billion in the expansion of its SiC capacity, a blot on the landscape has already formed in the shape of Huawei.

Following the US Bureau of Industry and Security (BIS) decision to add the beleaguered China tech giant to its 'Entity List', banning the business from buying components from US-based companies, Cree has updated its fourth quarter of fiscal 2019 financial guidance.

Based on the BIS decision and softer than expected demand for the company's LED products, the range of expected revenue from continuing operations has shifted from between $263 million and $271 million to the range $245 million and $252 million.

The lack-lustre LED product demand won't come as a huge surprise to most. When third-quarter results were released, chief executive, Gregg Lowe stated: "The LED market is experiencing softness... if needed we will shift manufacturing capacities to Wolfspeed should the LED market continue to soften."

Cree chief executive, Gregg Lowe, and Michael Baecker, Head of Volkswagen Purchasing Connectivity, during Volkswagen Group's FAST partner selection ceremony.

And as Lowe recently confirmed to *Compound Semiconductor*: "Our [$1 billion] investment won't impact our LED business... we have a fifty-fifty mix of GaN-on-sapphire and GaN-on SiC [LEDs] right now and we are moving towards sapphire-based LED products to free up SiC capacity for Wolfspeed."

But what will hurt more is the fact that revenue for products and materials associated with Huawei's wireless infrastructure build-out was expected to be up to $15 million in the fourth quarter of fiscal 2019.

In a general statement, the company said: "Pending any further guidance from BIS, [Cree] does not expect to ship any additional products in the fourth quarter for the Huawei build-out and cannot predict when it will be able to resume such shipments."

So what will be the impact of the BIS decision on Cree's SiC investment plans? When asked for comment, a Cree spokesperson simply said: "There is no impact on the expansion plan."

Indeed, in its latest financial update, the company alluded to the fact that it will be seeking to obtain licenses from BIS so that it can ship products to Huawei in the future.

And without a doubt, right now, Cree remains a formidable entity in compound semiconductor markets.

Acquiring the assets of Infineon Technologies' RF Power business last year has expanded Wolfspeed's offering of power and RF GaN-on-SiC products, and also bolstered the company's position against competitors such as Analog Devices and Qorvo.

The company's long-term SiC supply deals with ST Microelectronics, Infineon and an undisclosed third company – worth more than $500 million – clearly provide manufacturing security, with more to follow.

As Lowe has told *Compound Semiconductor*: "I would anticipate that sometime over the next year we'll have another couple of supply agreements in place."

And more recently, the Volkswagon Group selected Cree to join its 'Future Automotive Supply Tracks' initiative to accelerate technical innovations and drive vehicle projects forward. Other partners include Infineon and Osram.

"Volkswagon has something of the order of 50,000 suppliers of which only 67 are FAST suppliers – so we're in rarefied air... and they are excited about the capital expansion," said Lowe.

So against this backdrop, it becomes clearer how Lowe has managed to dramatically boost Wolfspeed's business by more than 100 percent in nearly two years, and could well continue to do so.

According to the chief executive, with the sale of Cree's Lighting products business now closed, the company now has some $1 billion in cash that will 'largely' fund the expansion across five years. During this time, two existing wafer fabs will be reconfigured into 'materials mega factories' while an existing structure will be built out into a 200 mm power and RF wafer fabrication facility.

The company intends to ramp manufacture of 150 mm wafers in 2022. But, importantly, come the mid-2020s, Lowe expects to convert production from 150 mm to 200 mm wafers, which coincides with anticipated increases in demand for electric vehicles.

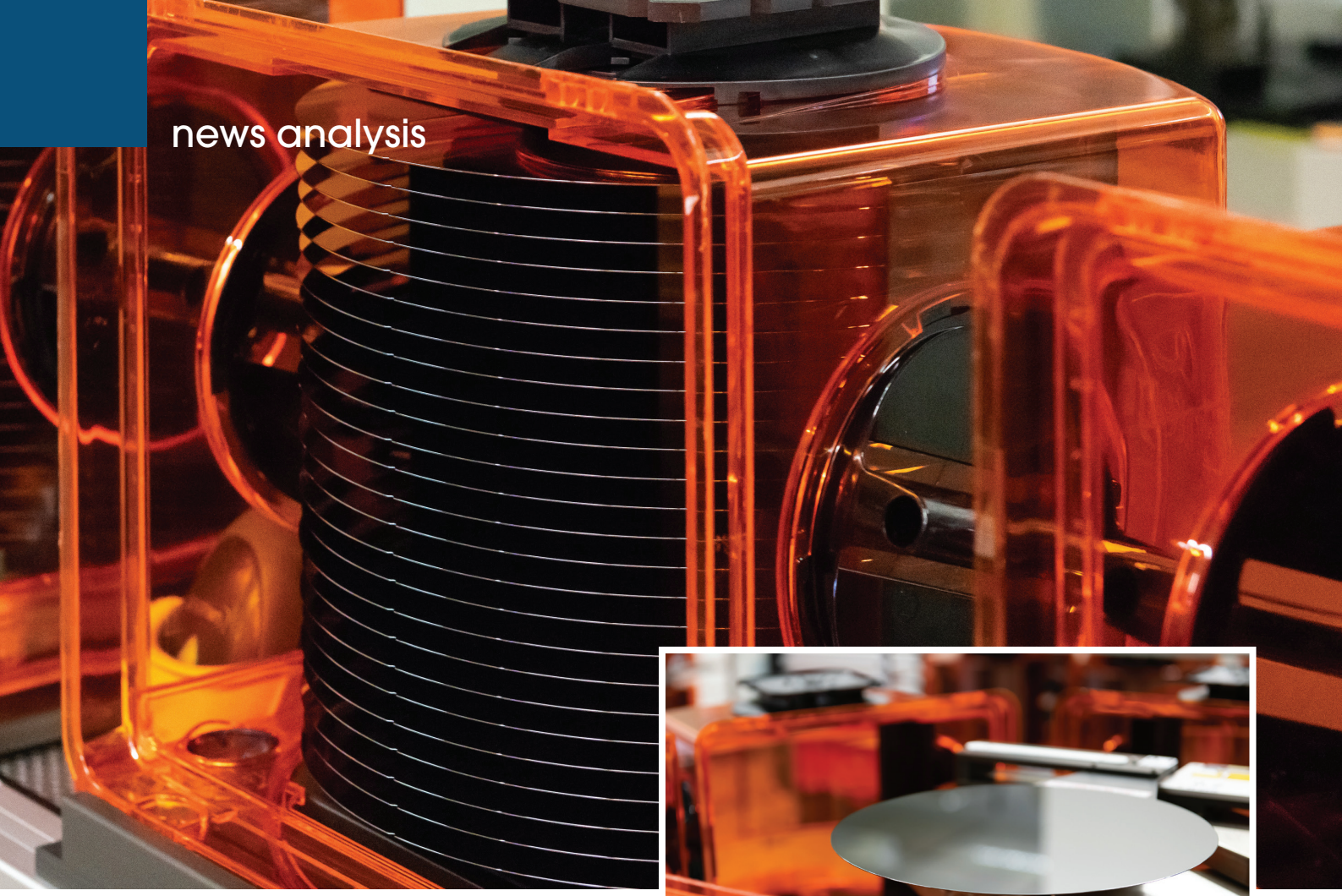
"The adoption rates of electric vehicles will definitely not be stable by 2024," says Lowe. "Right now less than 1 percent of cars are electric and between 2025 and 2030 most people think this figure will reach about 20 percent... that is going to be a pretty substantial ramp."

But rapid electric vehicle ramp or not, Cree is operating in a highly competitive landscape, clouded, at least in the short term, by the BIS ban on Huawei. Will Wolfspeed's bright future shine through?

On announcing the financial update, Cree's shares dipped by some 4 percent. However, within two days, share prices were bouncing back.

As Lowe put it: "When we announced the expansion at PCIM Europe [exhibition and conference] there was an audible gasp... and I believe this is the largest investment in the history of silicon carbide."

"Who knows what the competition is going to do," he added. "But in order for them to keep up they will have to invest one billion dollars and increase their capacity by thirty-fold... that's a pretty tall order."



Soitec:

Beyond silicon-on-insulator

Having just acquired EpiGaN, SOI manufacturer, Soitec, is set to take on 5G GaN power amplifier markets, reports Rebecca Pool.

JUST LAST MONTH, France-based manufacturer of silicon-on-insulator materials, Soitec, acquired EpiGaN, Belgium, for a hefty €30 million, adding to its growing suite of silicon-based and compound semiconductor technologies.

IMEC spin-off EpiGaN, has spent nearly a decade honing its GaN-on-silicon and GaN-on-SiC epiwafers. And as Soitec's head of strategy, Thomas Piliszczuk, puts it: "EpiGaN may be a start-up but the maturity of technology in their products is quite amazing, so with our support, we will be able move this forward very quickly."

Soitec span out of CEA-LETI, Grenoble, in 1992 to manufacture SOI wafers on an industrial scale using its wafer-bonding and layer-splitting process called Smart Cut. Here, ultra-thin insulating single-crystal layers are implanted into surfaces and then transferred from one substrate to another to produce a SOI wafer. Semiconductor manufacturers can then fabricate ICs onto the top layer of the SOI wafer to produce devices with, say, reduced parasitic capacitance.

Since this time, Soitec has continually ramped production, incorporated more materials into its Smart Cut process, including GaN, and today produces a range of engineered substrates for power and RF applications. For example, digital SOI products include a fully depleted SOI – FD-SOI – with an ultrathin top silicon layer on which to build low power chips for, say, base stations and handsets. Meanwhile, RF-SOI includes enhanced-Signal Integrity substrates with a trap-rich layer for LTE and LTE-Advanced front-end module ICs.

But while SOI products make up some 95 percent of Soitec's business right now – the company recently signed several long-term supply agreements for 300 mm SOI wafers with Global Foundries – it has been eyeing opportunities beyond SOI for some time. As Piliszczuk points out: "SOI is no longer a niche market and we have been growing more and more, so over the last few years we have made the first steps beyond SOI."

"For example, we develop engineering substrates using piezoelectric materials and are ramping up production of Piezoelectric on Insulator for RF filters while working with all the key RF companies," he says.

What's more, the company has honed it Smart Cut process to transfer a thin layer of crystalline material from a GaN or InP donor substrate to another substrate to produce a cost-effective compound semiconductor wafer. "We're engaged with key micro-LED makers to provide these substrates for devices and see huge opportunities here," says Piliszczuk. "We've been looking at GaN for some time and believe this technology has reached a point where it can bring in substantial business, especially for 5G."

But, Soitec doesn't intend to stop at GaN. According to Piliszczuk, the company has also been eyeing SiC opportunities for some time.

"Silicon carbide is a big opportunity and we are being pulled heavily by end-customers who believe we can bring lots of value here," he says. "Supply of silicon carbide is a huge challenge but with Smart Cut we could take a silicon carbide crystal, cut a thin layer and transfer this onto a [receiving] substrate and in this way generate a much bigger supply... so we are working very heavily on silicon carbide projects."

A future with EpiGaN

From here on in, EpiGaN is set to play a critical role for Soitec. Soitec's current line of SOI and POI products meet the demands of many of the key components critical to 5G base station and handset architecture, such as transceivers, low-noise amplifiers, antenna switches filters and more. However, with EpiGaN's GaN-on-silicon and GaN-on-SiC epiwafers the company can now make a play for power amplifier markets in both base stations and handsets.

Indeed, GaAs is currently the mainstream technology for power amplifiers in 4G and many 5G handsets, but GaN is making in-roads into 5G mmW markets. With EpiGaN, Soitec can also exploit this development.

"We first approached EpiGaN last year – we have a big offering of engineered substrates in 5G RF markets but also saw the big potential for GaN here too" says Piliszczuk. "We realised that by combining EpiGaN's technology with our market position and manufacturing scale would bring many opportunities."

With the acquisition secured, Soitec first intends to fully integrate EpiGaN into its company. As Piliszczuk says: "We will do this step by step but we want this to be the same business as Soitec."

The company then intends to ramp production at EpiGaN's production site in Hasselt, Belgium. Indeed, the former start-up recently purchased an Aixtron G5 reactor, which is currently being installed and qualified.

According to Piliszczuk, Soitec will add to this reactor, and also buy other process control and cleaning tools in the coming months. "There is enough space for additional tools and we are confident that we can use this space," he says.

And in a similar vein, Soitec will continue to move EpiGaN's epi-wafers from 6-inch to 8-inch production. "We want to make sure this project moves to the required level of maturity very quickly, and in the long-term we may need another production site," highlights Piliszczuk.

"RF 5G as well as power electronics markets are just growing and growing... but to a certain extent GaN businesses are vertically organised," he adds. "We believe this set-up is going to break, and our discussions with EpiGaN customers proves it – so we are confident we are now very well positioned to support these markets."

Colourful

chip-scale microLED displays

Patterning epiwafers with indium-rich InGaN quantum wells enables the fabrication of monolithic, full-colour displays

BY HOI WAI CHOI, WAI YUEN FU AND HAO LYU FROM THE UNIVERSITY OF HONG KONG

THE III-NITRIDE FAMILY has provided us with many great devices. Thanks to this material system, we have: blue LEDs, which power solid-state lighting; violet lasers, which lie at the heart of Blu-ray optical data storage systems; and HEMTs, which are well-suited for high-power and high-frequency applications. What will come next? There is a good chance it will be the microLED display.

The reason why this is a strong possibility is that GaN LEDs are already used in large outdoor colour displays, assembled from red, green and blue LED modules with millimetre dimensions. The size of these modules makes it difficult to diminish the overall size of the panels, or reduce the pitch of the pixels. However, if this could be done, these devices could target the huge market for indoor displays. That includes televisions and monitors, which are predominantly based on LCD panels. To compete in this market, the size of each pixel must be 100 μm or less. This is the domain of the microLED.

TVs based on microLEDs have tremendous promise. Prototypes already exist, such as Sony's 55-inch Crystal-LED, exhibited at CES2012, and Samsung's The Wall, a highlight of the recent CES2019. Merits of this LED-based technology include a display that is self-emissive, so unlike that based on liquid crystals, it does not require a backlight. Such a display also allows for great blacks, the key to extremely high contrast, by selectively turning off microLED pixels. That's a trait that is shared with OLED displays. However, microLEDs can switch faster, they cost less, consume less power, and are expected to be far more reliable in the long run.

The production of prototypes suggests that microLED displays are imminent. However, they might not be, given that there is yet to be a consensus on how they are to be built. Typically, red, green and blue microLEDs are fabricated at the wafer scale, before they are transferred to the display backplane with one of several techniques. Two of the most popular are 'pick-and-place' and 'mass transfer'.

Producing displays with this kind of approach is incredibly cumbersome, because so many red, green and blue LEDs have to be transferred to form a display. A full HD display requires 6 million LED chips, while four times this is needed to make a 4k display. These are massive numbers, on a par with the transistor count of the Pentium III microprocessor of the late 1990s. However, there is one crucial difference: those microprocessors were built using IC technology, with transistors monolithically integrated into a single chip using CMOS processes.

Assembling millions of individual LEDs to make a microdisplay poses many challenges. Targets must be met for yield, throughput, placement accuracy, performance uniformity and manufacturing efficiency. These are requirements that are particularly challenging for high-resolution displays for handheld devices, because the dimensions of the microLEDs are just a few microns.

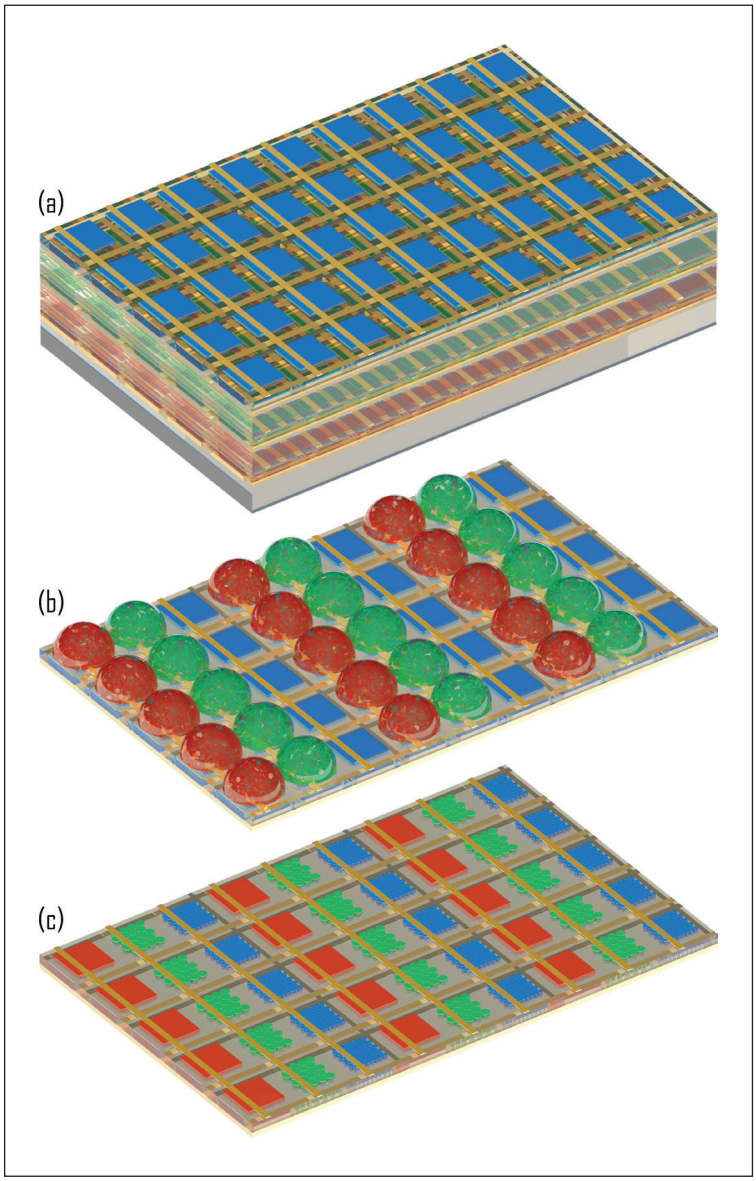


Figure 1. Schematics of proposed full-color microLED display by (a) stacking of red, green and blue microLED arrays, (b) selective phosphor coating, such as by jet-printing, on the red and green pixels of a monochromatic blue microLED array and, (c) monolithically integrating red, green and blue pixels on the same chip

One of toughest requirements for making a microLED display is to eliminate dead pixels in a cost-effective manner. At first glance, a transfer yield of 99.99 percent is excellent, but this still equates to more than 2000 dead pixels on a 4k display. That's simply unacceptable – the LCD displays of today have virtually zero dead pixels. Techniques for identifying and replacing dead pixels are being developed, but they contribute to manufacturing costs, reducing the chances of success in the hugely competitive display market. What's more, mass-transfer processes impose

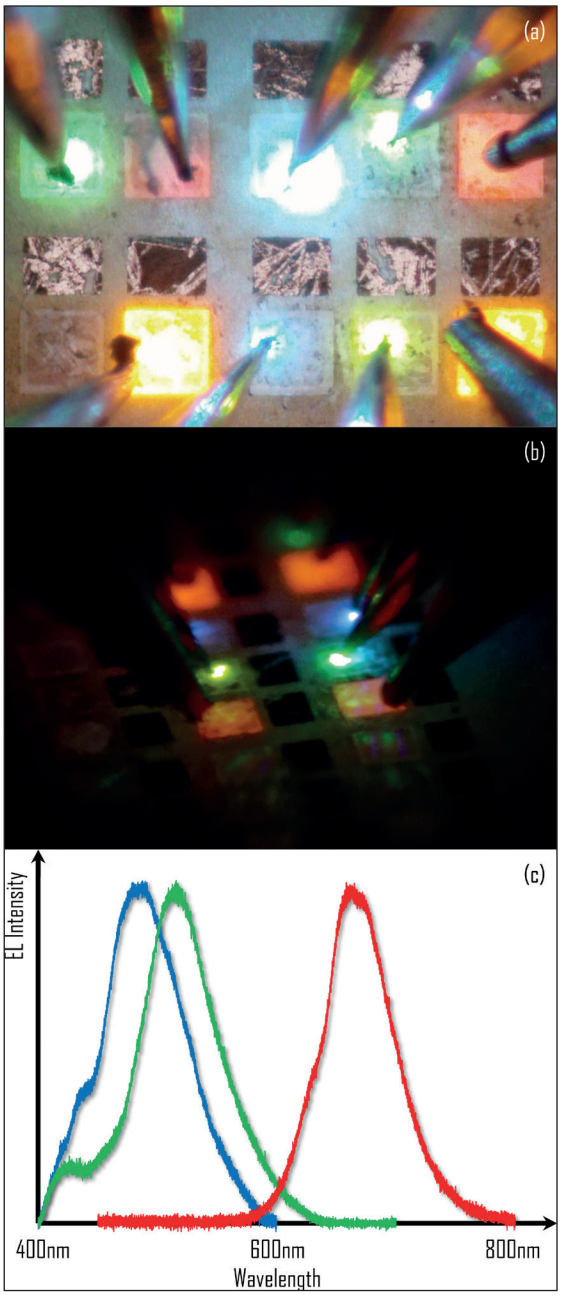


Figure 2. (a) Plan view and (b) isometric view photographs of a prototype for the monolithically integrated red, green and blue LEDs on the same GaN based LED wafer and (c) the corresponding electroluminescence spectra taken from the device.

a lower limit on the dimensions of the LED dies, and ultimately restrict the resolution of the microdisplay.

All these concerns highlight the need for a radically different production process, based on the use of IC technology for the manufacture of high-resolution GaN-based microLED displays. Adopting this approach would allow large numbers of devices and complex circuits to be batch fabricated on a single wafer, resulting in significant cost reductions as well as yield and reliability enhancements; the success of the silicon integrated circuits industry says it all.

If researchers pursue this approach today, they can draw on the development of microLED displays in the late 1990s. Back then, several research groups developed GaN microLEDs and microLED displays. These teams produced emissive microdisplays by forming monolithic arrays of micrometre-scaled LED elements, with pixels either addressed individually, or via a matrix. Being monolithic, such microdisplays are invariably monochromatic.

At the time, monochromatic microdisplays may well have been acceptable, as the mobile phones of that era often had mono-colour LCD displays. But now it's an entirely different matter. In fact, consumers are not just looking for a colour display, but one of high-quality, with a wide colour gamut, a high contrast ratio, a quick response time and high brightness. Since many screens are mounted on mobile handheld devices, there is also a premium on a low power consumption.

Working towards this is our team from The University of Hong Kong. We have developed various technologies, based on heterogeneous integration, that could deliver full-colour displays. One of our ideas is to stack red, green and blue microdisplay chips on top of one another to form a full-colour microdisplay (see Figure 1(a)); and another of our conjectures is to selectively coat the pixels in our monochromatic monolithic microdisplay using, for example, jet-printing (see Figure 1(b)). However, both of these designs require complex fabrication processes. Consequently, they are only a little more feasible than a mass-transfer approach.

To realise full-colour monolithic displays, the greatest challenge is the integration of multi-colour emitters from a single wafer. Sporadic reports have emerged of wafer-scale multi-colour emission, using various 'bottom-up' growth techniques. They include the growth of numerous sets of multi-quantum wells emitting at different colours within the same wafer, and the growth of nanostructures that feature either differing dimensions or different facets to generate various colours.

We tackle these fabrication issues from the opposite direction, pursuing a 'top-down' approach. Our starting point is the conventional planar GaN-on-sapphire LED wafer, which is compatible with conventional wafer process flows. On this we create nanostructures that induce spectral shifts. This enables us to generate colours that differ from that emitted by the multi-quantum wells. Ultimately, it allows us to make red, green and blue emitters that are monolithically-integrated onto the same chip or wafer.

The as-grown LED wafers that we start with produce single-colour emission, because the multi-quantum well structure is uniform across the wafer and the emission wavelengths from these wells are not tuneable. However, there is a possibility for bandgap tuning, arising from the highly-strained nature of the InGaN/GaN wells grown on *c*-plane sapphire. There is lattice and thermal mismatch during the growth of these layers, giving rise to the quantum-confined Stark effect, which is particularly prevalent in the indium-rich quantum wells that provide emission at longer

wavelengths. Through dimensional downsizing of individual emitters, emission can be blue-shifted via strain-relaxation. This can deliver substantial changes – we have produced spectral blue-shifts of more than 100 nm, by forming nanostructured emitters with dimensions of less than 100 nm.

Our strategy is to form the micro-sized red, green and blue pixels by patterning an LED wafer featuring indium-rich, red-emitting InGaN quantum wells. The red-pixels are non-structured, so they emit at the as-grown wavelength of the wafer. Meanwhile, the green and blue pixels are formed by creating densely-packed arrays of etched nanostructures that provide strain-relaxation. For the blue-light emitting structures, the dimensions are roughly an order of magnitude smaller than those for their green-emitting siblings (see Figure 1(c)). To speed prototyping, we patterning our green and blue pixels using selective nanosphere lithography. This involves the deposition of silica nanospheres onto photolithographically-defined photoresist wells, either by spin-coating or ink-jet printing. Wafer-level processing is possible, by turning to nano-imprint lithography.

We form our nanostructures by dry etching through the silica nanospheres. This creates nano-pillars, which are subsequently passivated and planarized using spin-on-glass. The quantum wells within these pillars undergo strain-relaxation, leading to emission at far shorter wavelengths. By interconnecting the red, green and blue pixels in a matrix-addressable format, we are able to construct a full-colour microLED displays at the wafer-scale (Figure 2(a) and (b)). There are no limitations on scalability.

Plotting the emission spectrum from our wafers reveals three distinct peaks at 487 nm, 516 nm and 667 nm, produced by blue, green and red pixels, respectively (see Figure 2(c)). This successful demonstration of monolithically-integrated red, green and blue emitters underscores the feasibility of our approach for chip-scale fabrication of full-colour microLED displays.

We have also developed a phosphor-free white-light LED, using a similar approach. Rather than grouping red, green and blue emitters as individual pixels, we randomly distributed them across the emission region of the LED to create a white-light source (see Figure 3). By generating white light without the need for fluorescence, this source avoids the use of phosphor coatings, which drag down the efficiencies and lifetimes of today's LED lightbulbs.

Of course, the proposed method is not without its drawbacks. Today's indium-rich InGaN epiwafers have a low quantum efficiency, holding back the performance of the devices. However, we believe that efficiencies will improve in the coming years. This will support the successful commercialisation of full-colour microLED displays that are based on the monolithic approach that promises to increase yield significantly and shorten the processing time.

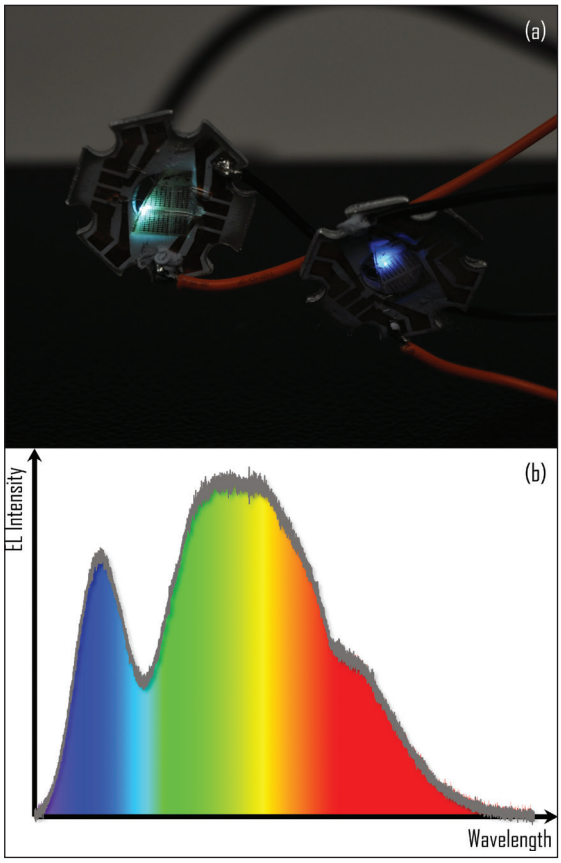


Figure 3. (a) Photograph of a phosphor-free white-light InGaN LED and (b) the corresponding electroluminescence spectrum

The monolithic integration technology that we have developed could also serve other applications. For instance, it could be used in a GaN photonic platform for on-chip communication, where fast microLEDs and photodetectors operating at multiple wavelengths could deliver a substantial hike in the data rates. This could be driven even higher with advanced multiplexing methods. Opportunities such as this make us very excited about the numerous functionalities and enhancements in performance that can follow from our development of microLEDs and their corresponding monolithic integration platform.

Further reading

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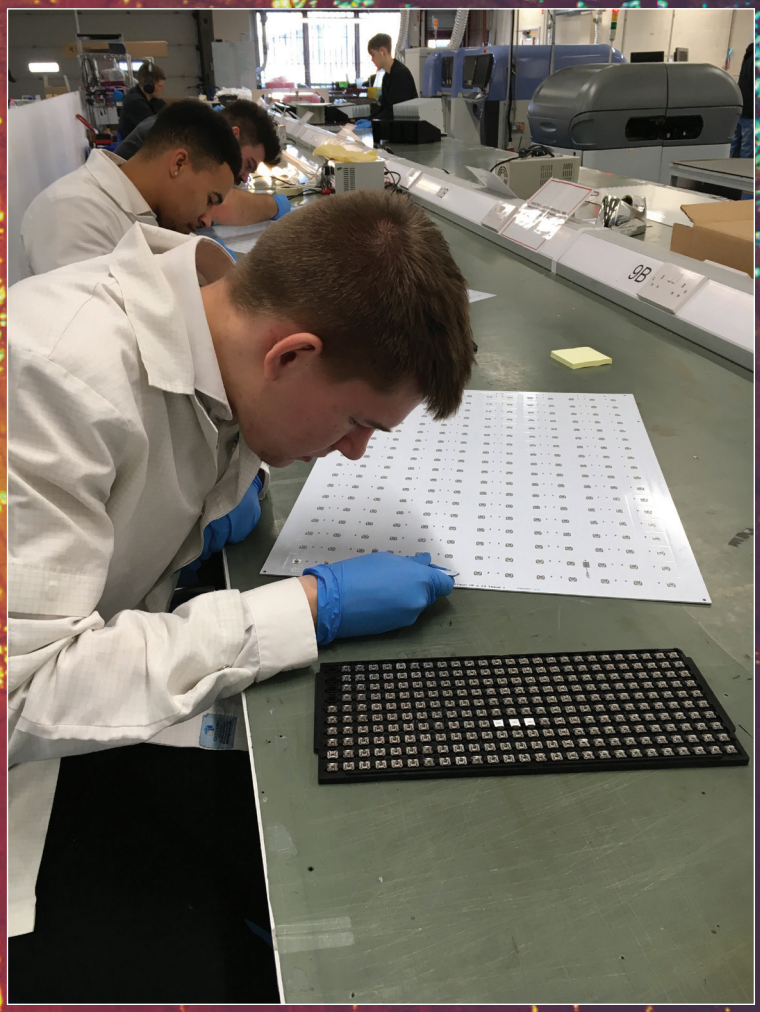
CPV: Boosting the bang-per-buck

Increasing concentration and streamlining production improves the capability of CPV

RICHARD STEVENSON REPORTS

RAISE EXPECTATIONS and optimism comes to the fore. But go on to dash these hopes, and what is left is a very bitter pill to swallow. Just ask those that have worked in the CPV industry. Their hopes soared at the beginning of the credit crunch, when manufacturers of silicon solar panels started fretting about the supply of raw materials. So great were those concerns that when these PV makers started to consume more material than the microelectronic sector, prices of the silcion panels ceased their steady decline. Instead, they headed north, setting alarm bells ringing. Could silicon ever reach grid parity? And could production of this technology ever reach a level where it could make a meaningful impact on the globe's carbon footprint?

Offering a solution came CPV. Leaping into the void were several start-ups promoting technologies that could generate a great deal of power from far less semiconducting material and a smaller land area than ever before. But before these firms really got going, silicon prices plummeted, killing off chances of significant success. Only a few hundred megawatts of CPV have ever been deployed, a figure dwarfed by that of silicon – to put volumes into perspective,

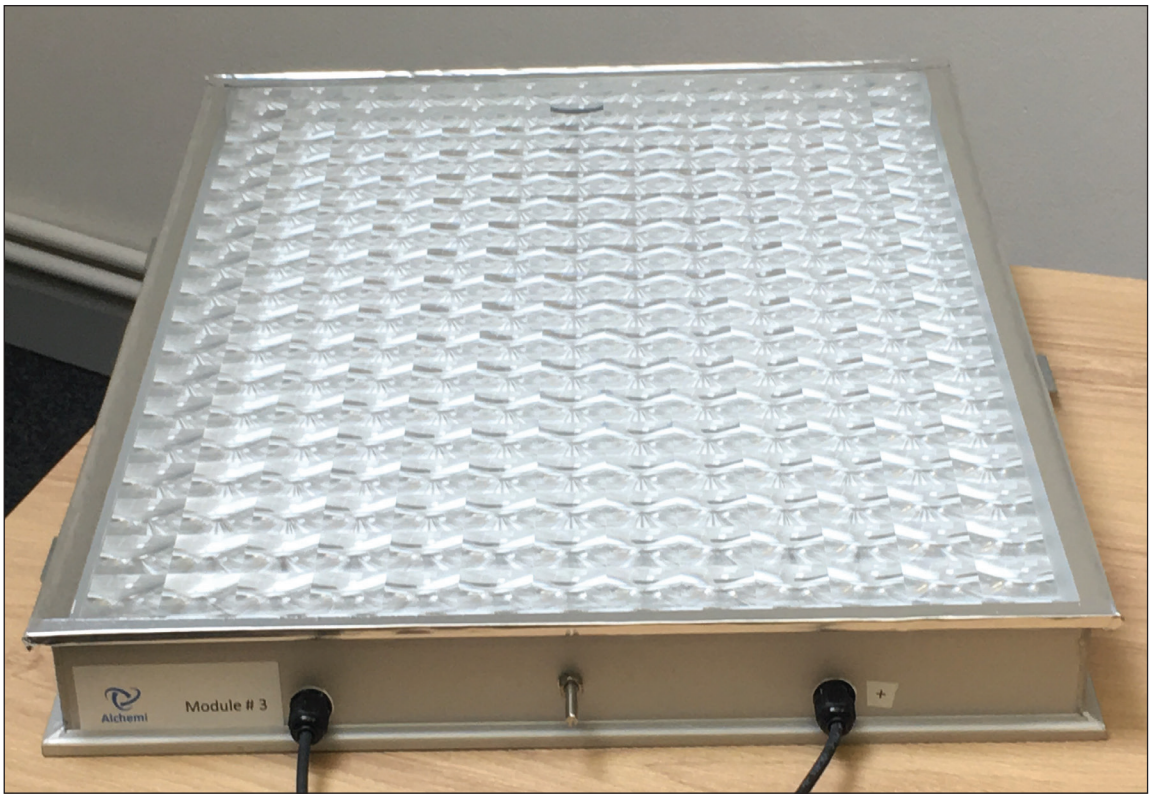


During the ALCHEMI project, cells are added to the module by hand. This can be automated for high-volume manufacture (image copyright PSL).

shipments of silicon panels now total more than 100 gigawatts per year.

So CPV is down – but it is by no means out, thanks to several on-going initiatives. Leading the way is the Canadian energy supplier STACE, which bought the CPV technology of Soitec. STACE continues to invest in CPV, having just established an operational production line. There is also Sumitomo Electric Industries, which is producing CPV systems that are generating electricity in northern Africa; RayGen of Australia, a user of multi-junction cells in systems that employ a vast array of mirrors to focus light on a relatively small area of a CPV receiver, to generate both electricity and heat; and several companies that are investigating micro-tracking technologies.

In Europe, where much of early CPV development took place, activity includes a three-year project entitled ALCHEMI – A Low-Cost, High Efficiency, Optoelectronic HCPV Module for 1000 Sun Operation. Through this programme a team is refining the performance of modules designed and developed by the UK-firm Fullsun. Other partners in this European



The CPV module is only about 55 mm-thick, thanks to the short focal length of the optical system. It is formed from a square silicone-on-glass Fresnel lens and a dome-shaped secondary objective that sits on top of the cell.

effort are IQE, Fraunhofer ISE, the Technical University of Madrid and the University of Cyprus.

"It's all about increasing the overall efficiency of the system and reducing the cost," explains project co-ordinator and spokesman, Andrew Johnson, who is IQE's Solar Business Unit Leader and Director of PV Technology. Primarily, the increase in efficiency and the reduced costs come from increasing the concentration on the cells from 625 suns to 1000 suns. Modules operating at this higher value have just been built, and are soon to be evaluated by several partners in the project, in both dedicated labs and outside, in sunny climes.

Much thought has been put into the design of the Fullsun module and how it is produced. The modules are much thinner than those made by the first generation of CPV firms, enabling a trimming of weight and material costs. Another attribute of the design is the use of very small cells, which are prevented from running too hot by dissipating their heat to the aluminium back plate. Manufacture is streamlined, using surface-mount technology and pick-and-place tools, replicating the approach taken in the LED industry. This allows outsourced production, avoiding the need for large capital investment in a dedicated facility.

Benchmarking success

The benchmark for the ALCHEMI project is Fullsun's first-generation module. Incorporating multi-junction cells with a 37 percent efficiency, it delivers a DC module efficiency of 30 percent. The target for the third-generation module – the second-generation got no further than the drawing board – is to raise the DC module efficiency to 37 percent using 41 percent cells. This will be realised while operating at 1000 suns.

One obvious question is why stop there? Would it not be better to move to an even higher concentration, and get an even better bang per buck? That's not unchartered territory – Semprius' modules operated at 1800 suns.

But right now, this could be a step too far. "The higher the concentration you go, the higher the pointing accuracy needs to be," says Johnson, who points out that heat dissipation also becomes more of an issue. In addition, the efficiency of the cell can pass its peak. "There will always be some series resistance issues in the epi-stack that will adversely affect the performance."

By operating at 1000 suns, the third-generation modules should avoid any overheating. "We have done some thermal modelling as part of this project, and it's clear that we don't have to worry about any extra heat sinking," explains Johnson. Calculations suggest that during operation, cell temperature should range from only 34 °C to 47 °C above ambient, a rise that is far less than that of a typical CPV module.

In the Fullsun design, two lenses are used to focus sunlight onto the cells. Light enters the module through a square Fresnel silicone-on-glass lens with sides of just over 30 mm. The light that leaves this lens is directed onto a dome-shaped silicone secondary

objective, which sits on top of the cell. Moving from 625 suns to 1000 suns requires a change to the optics. Due to project budgetary constraints, the team decided to realise this by simply modifying the Fresnel lens. This extended the focal length of the system from 43 mm to 49 mm, and led to a small increase in the thickness of the module – but, in relative terms, it is still thin.

The cells used in the third-generation modules are square, with sides of 1.3 mm by 1.3 mm. The optics focus the light to a spot that is just 1 mm by 1 mm, so there is contingency in the design. So, if there is any imprecision in focusing, which could lead to the spot wandering over an area of 1.2 mm by 1.2 mm, it is not an issue, as all the radiant power still impinges on the cell.

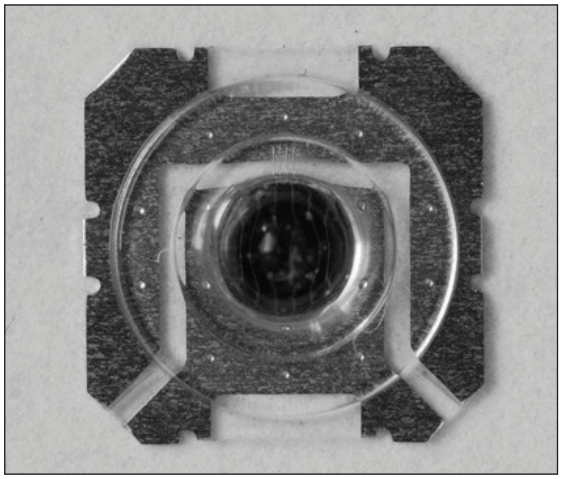
Evaluating architectures

To evaluate the most common multi-junction cell structures, the modules made in the ALCHEMI project have been populated with three different designs. Those that have been chosen have either a conventional architecture, an inverted metamorphic heterostructure, or an epitaxial stack that features a dilute nitride layer. IQE produced the epiwafers for the conventional design, with processing of the cells undertaken at the University of Madrid. The metamorphic design, containing cells based on GaInP, GaInAs and germanium, came from Azur Space Solar Power. Solar Junction provided the cells containing the dilute nitride, processing material supplied by IQE, which has an exclusive wafer supply agreement with this firm.

Flash tests provided a quick, insightful evaluation of cell performance. Normally, this test would be undertaken at around 1 sun, but for these measurements the incident power was 1000 suns. Results revealed the exceptional uniformity of the Solar Junction cells. 70 percent of them had an efficiency between 41 percent and 41.5 percent, and a further 20 percent had an efficiency in excess of 41.5 percent.

Such a high yield is valued for high-volume manufacturing. In this project, however, it's not necessary, as the wafer provides far more cells than are needed for the modules – and thanks to the insight provided by the flash test, just the best can be selected for use. To keep costs down, cells are added to the module by hand. However, if many modules were going to be made, assembly would be automated. Note that this does not require specialist robotic equipment, and could be carried out at many facilities within Europe.

Once the cells are on the modules, they are tested by biasing them, so they run as LEDs. Seeing if they glow offers a very quick route to identifying which cells are working.



A dome-shaped silicone secondary objective sits on top of the cell

Within each of the modules, there are by-pass diodes, which each sit alongside one of the 234 cells. Their role is two-fold. "If you have an array where you have shading, it's to keep the output stable," says Johnson. In addition, if the cells are wired in series, the diode prevents the failure of a single cell obliterating the output of the entire module.

Those in the project have built a total of ten modules. Recently, all of them were shipped to ISFOC, Spain, to undergo indoor testing. One will then remain there for outdoor testing, where it will be compared with a first-generation Fullsun module; another will go to Fraunhofer ISE, where it will be tested on-sun; and the remaining eight will be sent on to the University of Cyprus, where they can be benchmarked against some more of the original Fullsun modules and other PV technologies.

At the start of the project on-sun testing was scheduled to start at the beginning of this year. However, there have been delays, due to the procurement of the cells. That's not a big issue,

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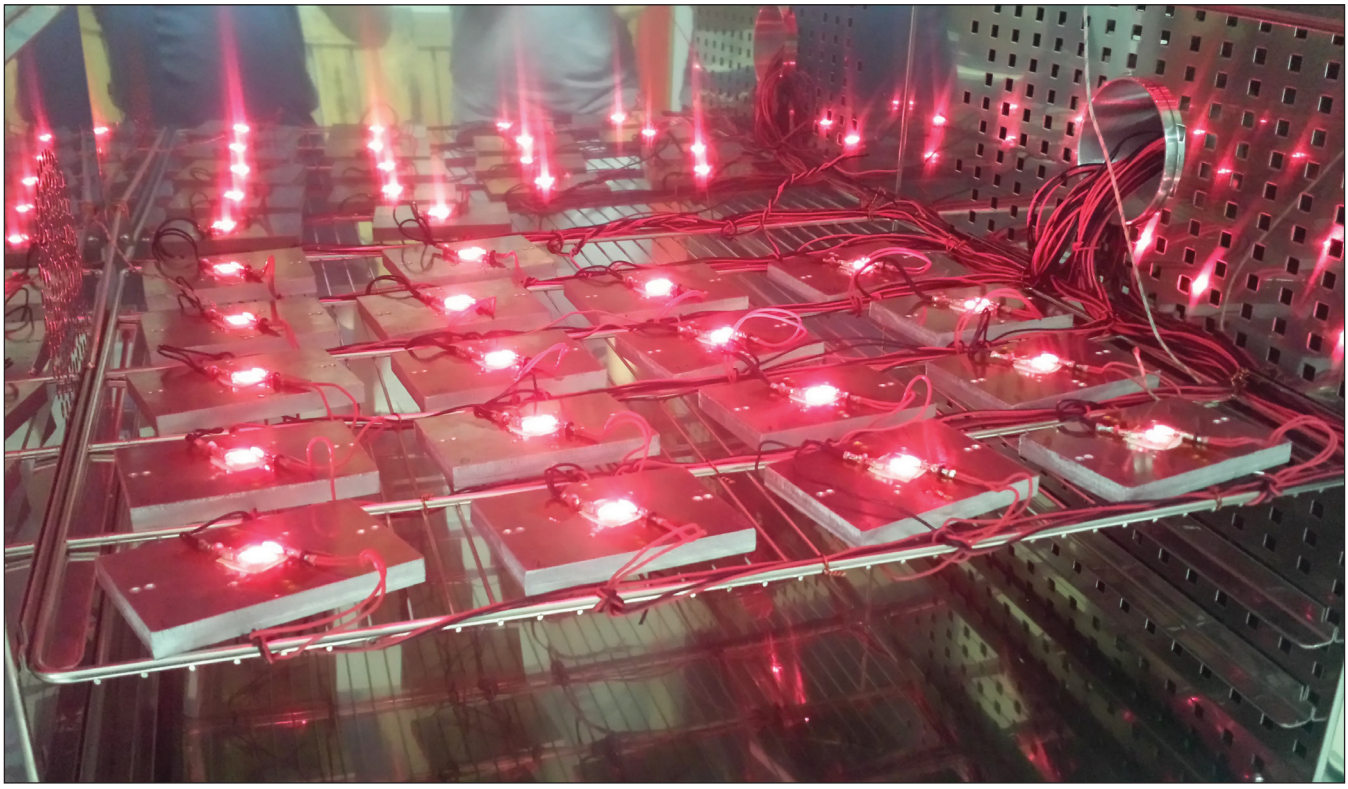
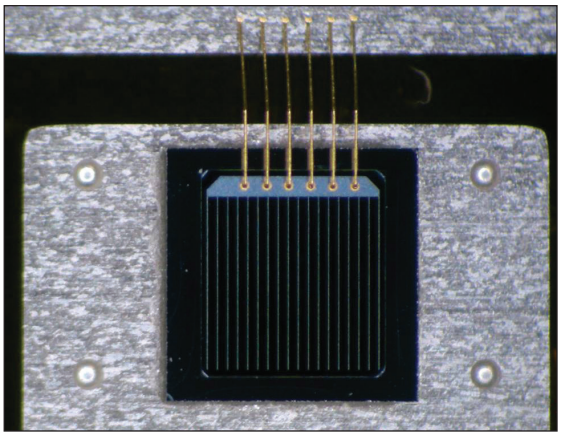


Evaluation of reliability included monitoring the performance of twenty encapsulated cells in accelerated degradation tests in climatic chambers

however, according to Johnson. "The reality is that by getting the modules on-sun now in Cyprus, it's probably the optimum time."

Testing of the modules should provide some insight into the values for the performance metrics. One of these is the cost-per-Watt, anticipated to be $0.90-per-Watt-peak, based on a roadmap of reducing manufacturing costs as volumes ramp.

A more valued metric is the levelised cost of energy. This is the energy that is produced, divided by the total system cost over the lifetime. It is a figure that must include factors such as the module performance change and lifetime, and the cost of maintenance, so at this stage, assumptions have to be made. The expectation is that the third-generation Fullsun technology could realise a levelized cost of energy of 0.04/ kWhr.



Power is transferred from the multi-junction cells by bonding gold wires, with a thickness of 25 μm, to these devices.

A bright future for CPV?

Even though costs are coming down, it is hard to see CPV making an impact in the next few years. But there are signs that it could do further down the line. Johnson is seeing a reduction in the number of suppliers of silicon cells and modules, and that might start to apply the brakes to price declines.

In contrast, the cost of CPV cells could fall dramatically, due to growth in the shipments of multi-junction cells to makers of satellites. Although cells for satellites differ from those for CPV, the changes are minor, and any reductions in cost are easy to transfer.

Taking the space PV market to a new level is the deployment of mega-constellations of satellites. Programmes include Space X, One Web, and Amazon Kuiper, with latter planning to put 3000 satellites into low earth orbit to provide internet connectivity across the globe.

"Most of these satellites will have a short finite lifetime, maybe five years, and then they have to be replaced," says Johnson. "So it will significantly drive the cell volumes, and obviously there will be pressure to reduce cell price, which can only help CPV in the long-term."

Only time will tell if these cost reductions are big enough to drive a resurgence in CPV, and ultimately spur significant deployment. Demand for green energy is only going in one direction, so there's hope. However, let's not raise expectations too high.

Making improvements with **multiple materials**

Better products result from etching GaN diodes from native substrates, uniting GaN HEMTs with passive devices formed on high-resistivity silicon, and growing III-Vs on silicon

BY RICHARD STEVENSON

NO-ONE LIKES to compromise. It feels far better to select exactly what you want, rather than being constrained by your choices.

But in our industry, compromise is a common occurrence. You may crave the high power densities of GaN, but bemoan the low thermal conductivity of this wide bandgap material; or need the long-wavelength capability of the antimonides, but despair at the lack of maturity of this material system for high-volume production.

To improve this state of affairs, much effort has been directed at combining different semiconducting materials. This allows the merits of one to be allied with the strengths of another. Compromises still have to be made, but one gets far closer to the ideal.

Highlighting the gains that are possible with this approach are a handful of talks that were delivered at this year's CS Mantech, held at Minneapolis, MN, from 29 April to 2 May. Speakers on this theme included Chris Youtsey from Micolink Devices, who revealed how cost-savings and superior thermal management result from removing GaN *p-n* diodes from their native substrate and transferring them to a copper carrier. In addition, Sangmin Lee from Wavice outlined how to use high-resistivity silicon as a foundation for integrated passive devices and GaN power amplifiers; and Amy Liu from IQE detailed how epitaxy can unite the low-cost, scalability and high level of integration of silicon with either the optical properties of InP and GaSb, or with the RF attributes of InP.

Reducing thermal impedance

The recent emergence of the large diameter, GaN substrate has spurred much effort in the development of vertical, GaN-on-GaN devices. Compared with those made from silicon, GaN-on-GaN diodes and transistors with this geometry promise multi-kV switching at far faster speeds and a substantially reduced on-resistance.

Off-setting these strengths, the GaN substrate has two major drawbacks. It is very expensive, hampering the commercial success of this technology; and it has a high thermal impedance, limiting the maximum power density and leading to larger die.

Addressing both these issues are Chris Youtsey and his co-workers from MicroLink Devices, working in partnership with engineers from Qorvo, Virginia Tech and the University of Notre Dame. By etching devices from the substrate and mounting them on copper, these researchers mitigate high production costs through substrate re-use; and they lower thermal impedance by attaching the chip to a copper carrier. Youtsey believes that the re-use of the GaN substrate could enable substantial cost savings. "I think at least three to five reuses is possible. There is a cost associated with re-polishing GaN, but this will be a fraction of the cost of a new substrate."

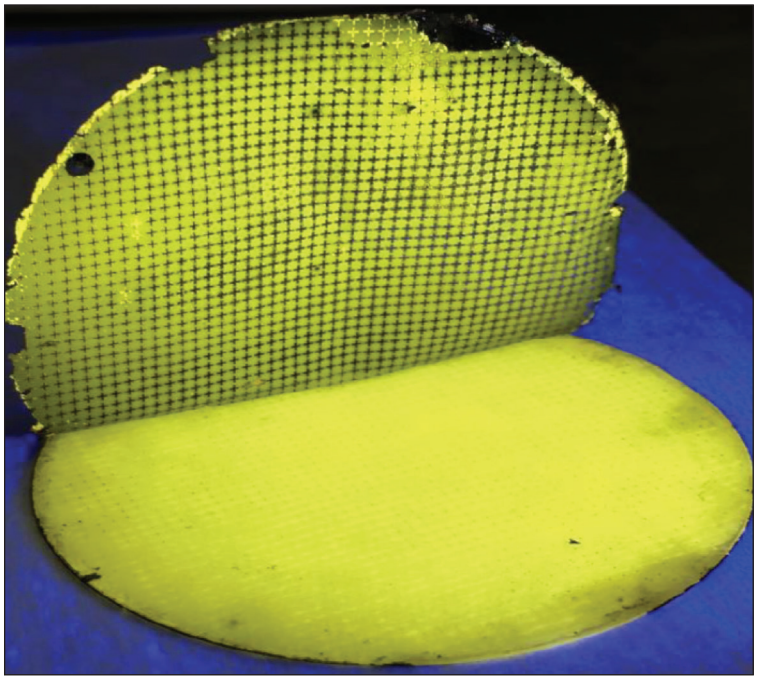


Figure 1. The team at Microlink have developed a photoelectrochemical etching technique that can remove a GaN epitaxial film from a 2-inch GaN bulk wafer.

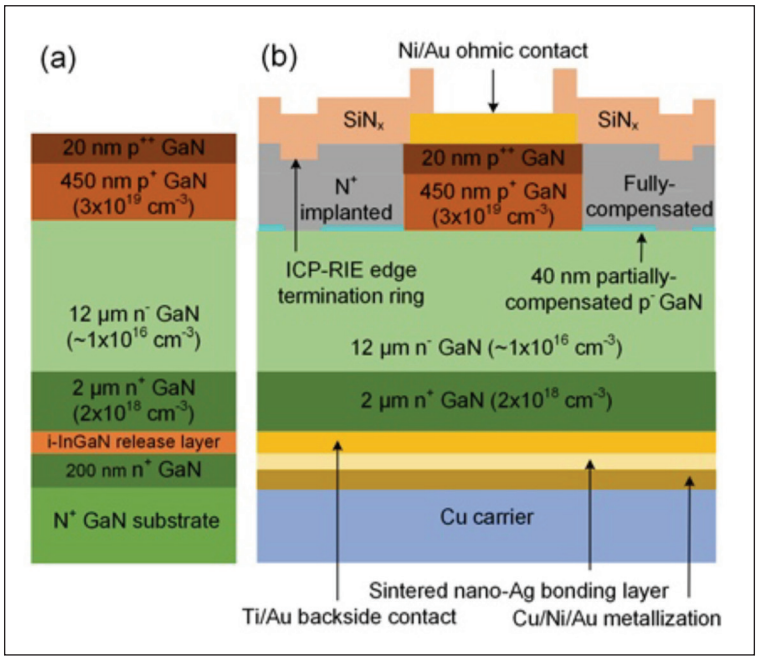


Figure 2. Microlink improves the thermal management of its GaN *p-n* diodes by bonding them to a copper carrier.

He and his colleagues have spent many years developing and refining their photoelectrochemical technology for removing device structures from substrates (see Figure 1). However, it is only recently that they have applied this technique to the challenging task of separating a GaN device from its native foundation. "These [devices] require very high

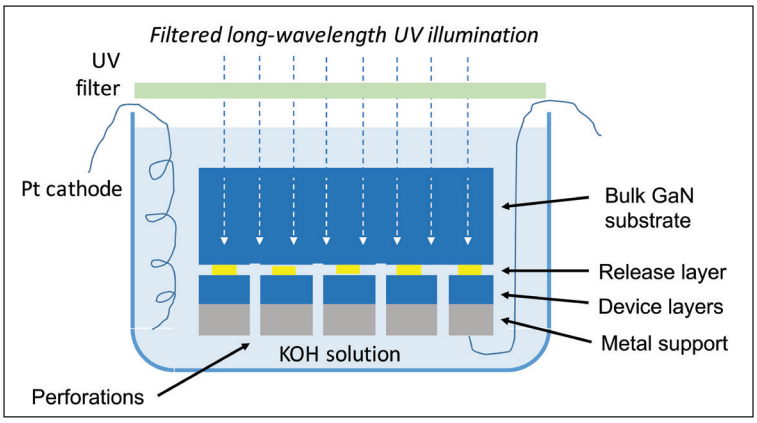


Figure 3. For the photoelectrochemical etching process, Microlink's engineers use a platinum cathode. The sample acts as the anode.

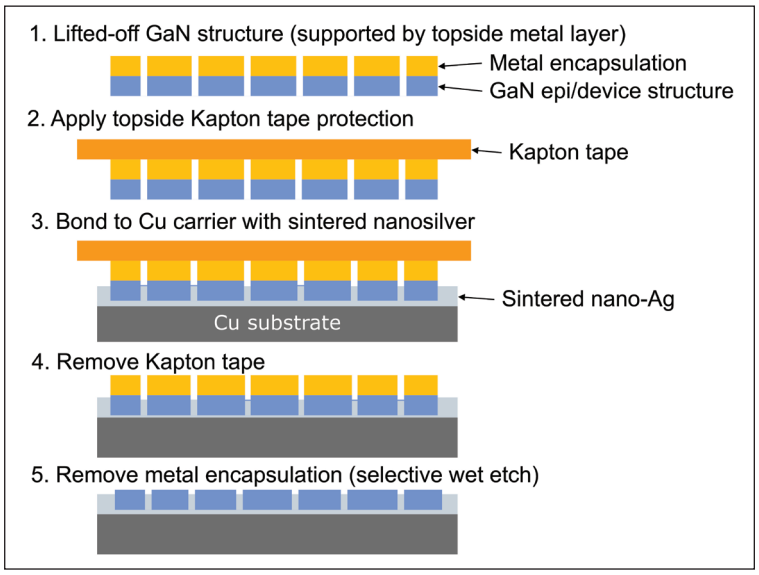
material quality and advanced device processing, incorporating effective edge termination, to achieve a low leakage current and a high breakdown voltage," explains Youtsey.

Comparing the performance of the *p*-*n* diodes produced with this technique with those with a conventional architecture reveals that both designs have a nearly identical blocking voltage and ideality factor. However, the thermal impedance is cut by 30 percent with the transfer to the copper carrier.

"Note that the thermal benefits of epitaxial lift-off may be even more compelling than substrate re-use, since the layer transfer enables higher performance and reduced die sizes," argues Youtsey.

Figure 4. Micolink's process flow for layer transfer and bonding of the released GaN foil.

The fabrication of the team's diodes begins by loading HVPE-grown GaN substrates into an MOCVD chamber and depositing a sacrificial layer of un-doped InGaN, followed by a device heterostructure (see Figure 2). To support high-voltage operation, the engineers realise edge termination, using a shallow trench etch and a triple nitrogen implant. Evaporation and subsequent annealing at 600 °C adds low-resistance *p*-GaN ohmic contacts, and passivation results from the sputtering of silicon nitride. Evaporation of metal on the backside provides the *n*-type contact. For the control, the researchers use a Ti/Al/Ni/Au stack on the back of the wafer, while for the diode removed from the substrate, they use Ti/Au. Before starting the removal process, devices are encapsulated by sputter-depositing a TiW-Au seed and adding a 25 μm-thick support layer by electroplating. "Plating this thickness is not a major cost driver – maybe a few dollars per wafer," says Youtsey.



Cross-shaped perforations are then defined in the metal support layer, and etched through the heterostructure to the release layer using wet and dry etching. To remove the sacrificial layer, the structure is placed in a beaker filled with a potassium hydroxide solution, with platinum and the sample used as the cathode and anode, respectively (see Figure 3). Etching frees the device when UV light is illuminated through the bulk substrate and absorbed in the InGaN release layer.

After forming the released GaN foil, the *n*-type contact is blanket evaporated on the nitrogen face, before Kapton tape is applied to the top surface of the metal support layer (see Figure 4). The copper carrier is attached to the structure with a sintered nanosilver paste. After annealing at 260 °C for an hour, this forms a robust bond with high electrical and thermal conductivity. Finally, the Kapton tape is peeled off, before the metal encapsulation layer is removed by selective wet-chemical etching to the device structure.

Although quite a few steps are required to produce these devices, Youtsey believes that the additional processing is "not overly burdensome", and he argues that it is justified by the benefits. He also points out that streamlining would take place before the technique entered production.

To support his claim for the suitability of the technique within a fab, he remarks that even with a conventional die-attach process, a full-thickness GaN substrate would have to be mounted on a temporary carrier, prior to backgrinding and the addition of a backmetal contact – and then there would be demounting, remounting to a tape frame, dicing, pick-and-place and die attach. With the technique he and his co-workers have pioneered, there is no need to backgrind, and dicing is simple, due to the thin foil that is held together by "tabs". According to Youtsey, the additional process steps associated with the epitaxial lift-off process involve primarily etching away the metal encapsulation.

Measurements of the diode on the copper carrier and the control show that both have an abrupt breakdown voltage at 1.3 kV, with failure stemming from imperfect edge termination, rather than defects within the diode region. The current-carrying capacity of the novel diodes exceeds that of the control. Those with

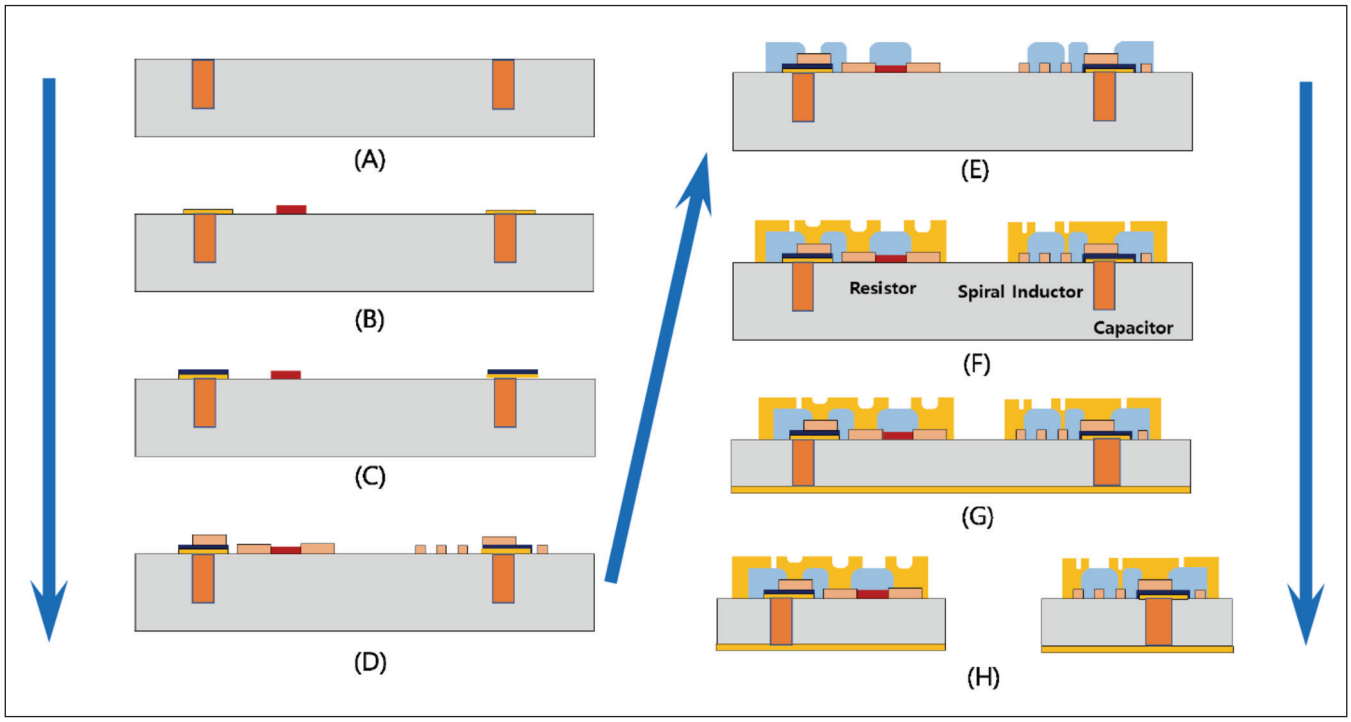


Figure 5. Wavice employs the following process flow for forming integrated passive devices on high-resistivity silicon with a via first, through-silicon-via process: (a) trench etch and copper fill, (b) NiCr resistor (red) and metal 1 (yellow), (c) SiN dielectric layer, (d) metal 2, (e) passivation, (f) metal 2 interconnect, (g) back grinding and metallisation, (h) singulation.

diameters of 324 μm and 550 μm can pass 6.5 A and 10 A at a forward bias of 5 V. In comparison, at the same bias the control needs a diameter of 1 mm to pass 10 A, highlighting the potential for die reduction with the photochemical etching process.

To assess the prospects for substrate recycling, the team reclaimed GaN substrates that had been used to make devices, and, in collaboration with Sumitomo Electric, removed about 50 μm of material with chemical mechanical polishing. Forming a *p-n* diode on this foundation and evaluating its performance with current-voltage plots shows that its behaviour is very similar to that of a device grown on a prime substrate.

Youtsey believes that the team's technology has now reached critical mass, due to demonstrations of feasibility. "We are now engaged with several device manufacturers, and are actively looking for additional partners, with whom we can further develop and transfer the process into production." According to him, the process has the potential to be used in the production of LEDs, microLEDs, VCSELs, photodiodes, laser diodes, and vertical power electronics.

Compact, powerful amplification

The roll-out of 5G infrastructure requires power amplifiers with a high output power, high linearity, high efficiency, low cost and small form factor. Although these performance criteria can be met with GaN MMICs, they are pricey, while the use of printed circuit boards fails to fulfil the need for a small footprint.

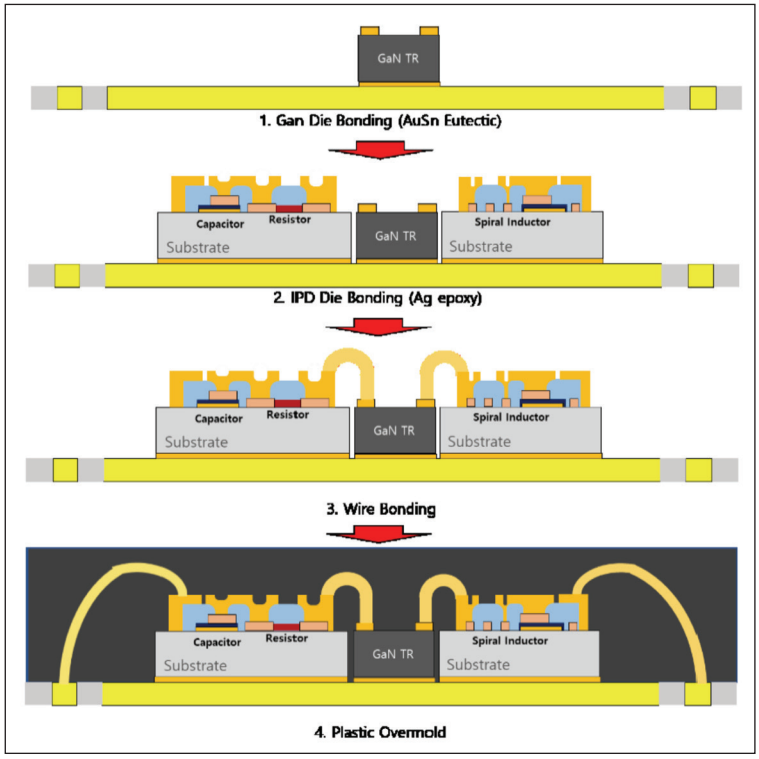


Figure 6. Wavice's process flow for making quasi-MMICs by the hybrid integration of GaN HEMTs and integrated passive devices.

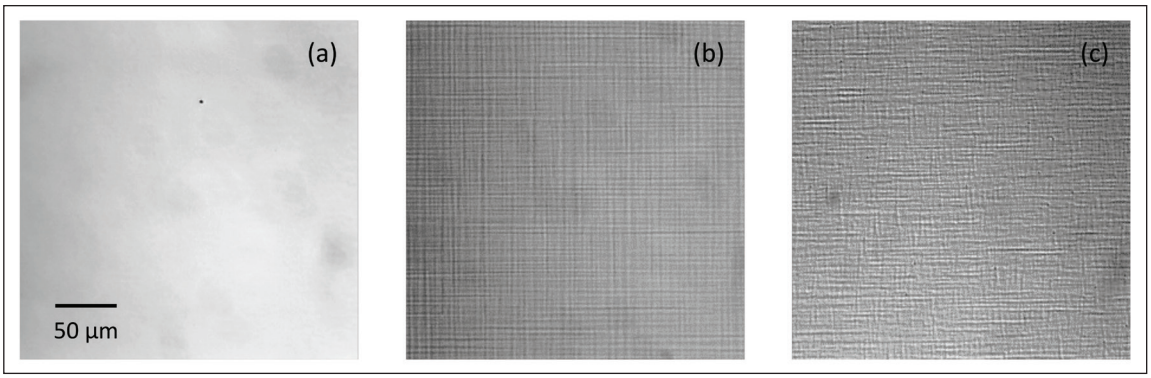


Figure 7. Normaski images of InP resonant-tunnelling diode structures grown at IQE. Images are for the devices structures grown on: (a) InP, (b) GaAs, and (c) and germanium-on-silicon.

One promising alternative is the construction of quasi-MMICs, formed by hybrid integration of low-cost integrated passive devices and high-power amplifiers. Reports of this type of approach have emerged from universities, and now a manufacturing facility is following in these footsteps. Engineers at Wavice, Korea, have found by using this technology to surface mounting components on a board, they can slash the footprint for the unit from 30 mm by 30 mm to just 8 mm by 8 mm.

The starting point for this work is 525 µm-thick silicon substrates with a high-resistivity, because this trims the RF transmission loss. "It is standard, cheap, high-resistivity silicon," says team spokesman Sangmin Lee. "We didn't use high-purity, high-resistivity silicon."

On this foundation Lee and co-workers create a 120 µm-deep trench, and fill it with electroplated copper, using TaN as a diffusion barrier. The purpose of this trench is to provide a through-surface via after the wafer has been thinned by back-grinding.

The next steps involve the addition of a silicon nitride film by plasma-enhanced CVD, followed by the creation of a NiCr resistor by sputtering and conventional lift-off. On this they add several metal and insulating layers, so that they can create capacitors between the first and second interconnect metals, and inductors between the second and third (see Figure 5).

The backside of the wafer is then ground to a thickness of just 100 µm. This serves two purposes: it exposes the copper filled trench; and it ensures that the height of the integrated passive devices is the same as that of the HEMT. Integrated passive devices and HEMTs are then attached to the package base metal with a AuSn eutectic and silver, respectively (see Figure 6).

For the work reported in the CS Mantech paper, the team used a Wolfspeed CGH60008D for their GaN HEMT. Note, however, that Wavice also makes its own HEMTs. Its business model is to allow customers to choose between in-house HEMTs and those produced and by other suppliers.

Measurements on the package containing the Wolfspeed transistor reveal a peak power of 40.5 dBm. "It is about the maximum power from the device, which means no loss from the packaging," says Lee. During his conference talk, Lee showed the results of an X-band FET, featuring wafer-level packaging, high-resistivity silicon and a Wolfspeed CGHV1J0780D. That unit produced 52 dBm at 10 GHz. Lee says that higher powers are possible, but describes this level of performance as "reasonably good".

The team are undertaking reliability testing of some of their quasi-MMICs. Assuming that the results are encouraging, the plan is for this technology – integrated passive devices on high-resistivity silicon – to be added to the company's foundry service. Additional goals include developing high-power amplifiers producing between 5 W and 30 W in the 2-6 GHz range, and a linear power amplifier with an average power of 5-10 W.

III-Vs on silicon

The most attractive, but most challenging approach to uniting the III-Vs and silicon is epitaxial growth. Enjoying success is not easy, as there is a need to address lattice mismatch, while supressing the formation of anti-phase domain boundaries.

The most attractive, but most challenging approach to uniting the III-Vs and silicon is epitaxial growth. Enjoying success is not easy, as there is a need to address lattice mismatch, while supressing the formation of anti-phase domain boundaries

Doing just that is epiwafer supplier IQE, and at CS Mantech the company's Amy Liu – who works at the Bethlehem, PA, site – offered an overview of the growth process the company has developed.

For this work, IQE uses (100)-oriented silicon substrates with a 6° off-cut toward [111], because this helps to supress the formation of anti-phase boundaries when the polar III-V material is deposited on non-polar silicon. Its other initiative to ease the transition from silicon to the III-Vs is to use a germanium transition layer, which has a similar lattice constant to that of GaAs.

The germanium layer is grown by CVD in an ASM E2000. Engineers then tend to switch to a Veeco GEN2000 multi- 6-inch production tool to add the GaAs layer, before transferring this epiwafer to either an Oxford-VG V-100 or V-150 production MBE system for the growth of the metamorphic buffer and the device layers predominantly based on InP.

Note, however, that it is possible to do this type of work by MOCVD. "We have demonstrated MOCVD growth process for InGaAs quantum well FETs on silicon, so we should be able to replicate other InP based devices also," says Liu, who points out that the choice between MBE or MOCVD is governed by which growth process is best suited to creating the active device structures.

One of the structures that Liu and her co-workers have grown on silicon is an InP-based resonant-tunnelling diode. This class of electronic device is faster than any other, making it a promising candidate for use in energy-efficient, compact, ultra-broadband, short-range wireless communication. In such systems, the resonant tunnelling diode could be used as a receiver.

Supported by the EU project iBROW, the engineers at IQE have made resonant-tunnelling diode structures with an InGas/AlAs double barrier quantum well that feature an InAlAs metamorphic buffer, linearly graded to a high indium content.

The increase in lattice mismatch required to produce these InP-based structures led to strain relaxation. Epiwafers exhibit a slightly elevated surface roughness and a degree of cross hatching (see Figure 7). However, despite this degradation in morphology, this material is still able to produce resonant tunnelling diodes with their hallmark negative differential resistance.

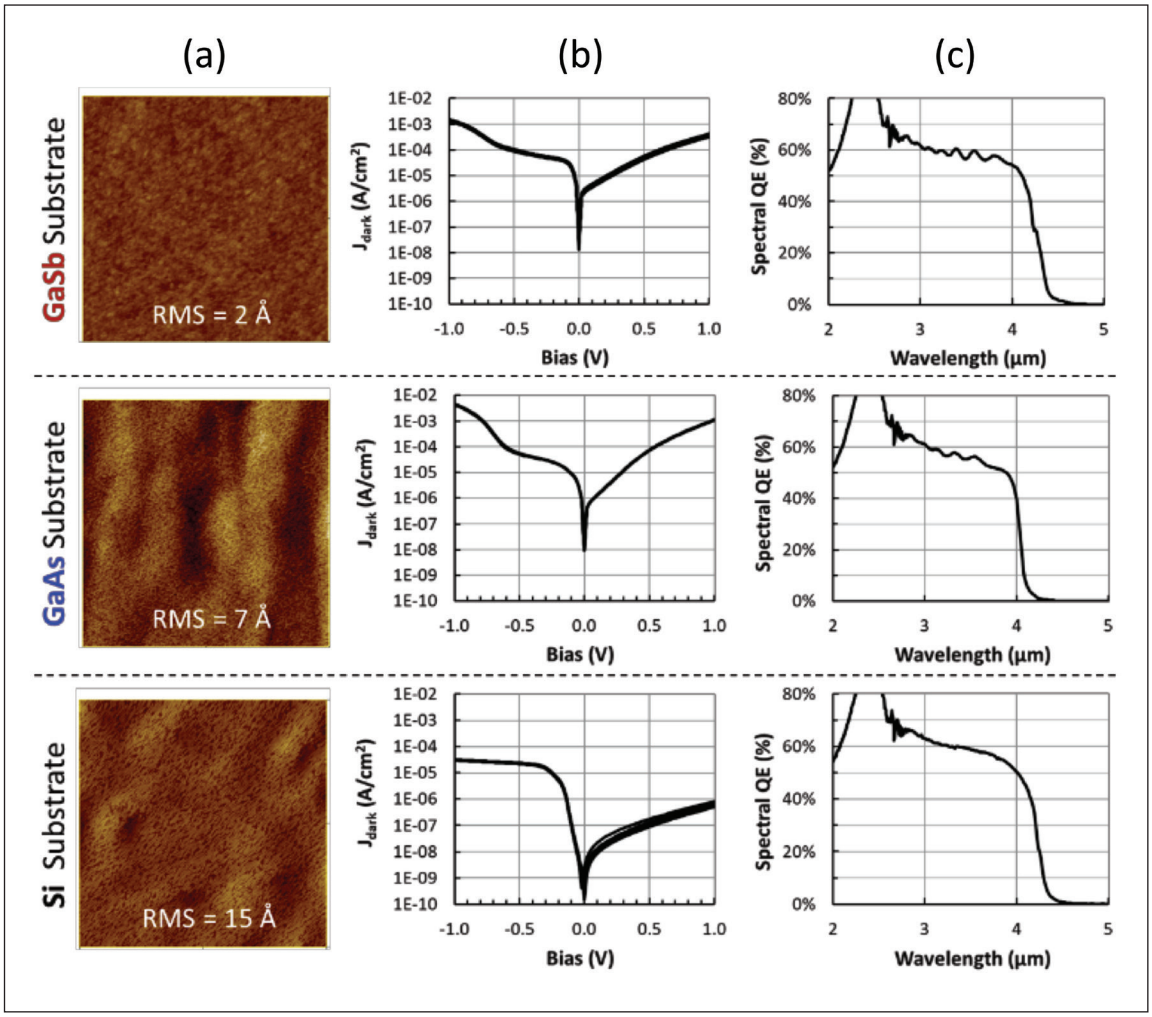


Figure 8. Engineers at IQE have grown the heterostructures for GaSb infrared photodiodes. Comparisons of atomic force microscopy images (a), current-voltage plots (b) and spectral response curves (c) are made for devices grown on GaSb, GaAs and silicon substrates.

Figure 9. An infrared image taken from a focal plane array fabricated from an antimonide-based medium-wave infrared structure grown on a germanium-on-silicon template. The inset shows the corresponding visible image.

Liu and her co-workers have also produced quantum cascade lasers. According to this team, this class of device delivers the highest performance in the entire medium-wave infrared and long-wave infrared spectral range. Constructing it on a silicon platform could open the door to low-cost, ultra-compact quantum cascade lasers for wireless communication, sensing and illumination.

At IQE, engineers have fabricated quantum cascade laser structures with 40 stages, each incorporating strained AlInAs barriers and InGaAs wells. The team had previously fabricated this structure on a GaAs substrate, with processed devices realising room-temperature lasing at 4.4 μm. Switching to a silicon substrate has proved challenging, partly due to the high degree of strain in the structure. The active region is designed to balance the internal forces, but the strain in the individual layers and any net residual strain adds to growth challenges.

Studying the surface morphology at various stages of growth revealed that this deteriorated with the addition of the active region. As one would expect, device performance and yield were impaired. However, these emitters were still able to deliver lasing at up to 170K.

After growing the resonant tunnelling diodes and quantum cascade layers, Liu and her colleagues started to see if they could improve the quality of the underlying germanium. They estimated that the threading dislocation density in the germanium is in the mid 10^7 cm^{-2}, and they thought that the threading dislocation density in the InP layers would be about ten times this figure.

The traditional approach to determining the threading dislocation density is to inspect the material with cross-sectional and plan-view tunnelling electron microscopy. This is not ideal, however: it is time consuming, costly, the inspection area is limited, and it is unreliable when the threading dislocation density drops below 10^7 cm^{-2}. To address all these issue, IQE's silicon division has developed an in-house, wet-etching metrology technique. "It uses a proprietary etchant chemistry to effectively, easily, and quickly reveal etch pits on the germanium-silicon templates," says Liu. According to her, the density determined by this technique correlate well with transitional threading dislocation density measurements, such as transmission electron microscopy.

Using this in-house wet-etching metrology technique to assess threading dislocation density, Liu and co-workers undertook a programme to improve the quality of the germanium layer. Following several process modifications, this density fell to typically 5×10^5 cm^{-2}.

The team have used the refined growth process to produce medium-wave infrared photodetectors, based on building GaSb structures on silicon substrates. This effort draws on previous work, involving the growth of metamorphic GaSb-based devices on GaAs substrates with a similar cut-off wavelength. When these structures were grown on 6-inch GaSb and GaAs substrates, they exhibited mirror-like surfaces, with roughnesses of 0.7 nm and 0.2 nm, respectively, according to atomic force microscopy. Switching to a silicon substrate led to a higher density of mounds, and an increase in surface roughness to 1.5 nm (see Figure 8).

However, even this increased roughness is acceptable for device fabrication. Detectors made from this heterostructure had a slightly higher dark current than equivalents incorporating the other two foundations, but they had a similar quantum efficiency – it's 60 percent, even without an anti-reflection coating.

The structure on silicon has been fabricated into a focal plane array with 640 pixels by 512 pixels at QmagiQ of Nashua, NH, using a 15 μm-pitch process. Applying an anti-reflection-coating and moving to a fully packaged array propelled the quantum efficiency to 80 percent, with operability close to 100 percent. This is a level of performance able to provide high-quality imaging (see Figure 9).

One of the next goals for the team is to grow the InP-based resonant-tunnelling diodes and quantum cascade lasers on the improved germanium-on-silicon templates. This should lead to an increase in device performance.

"We also plan to continue our work on antimonide-based, infrared photodetectors on germanium-on-silicon templates, extending the work to longer wavelength devices," explains Liu.

Such efforts will continue to showcase what is possible by uniting different material systems. It's an approach that is not the norm today, but it's becoming more common, and this trend seems set to continue.

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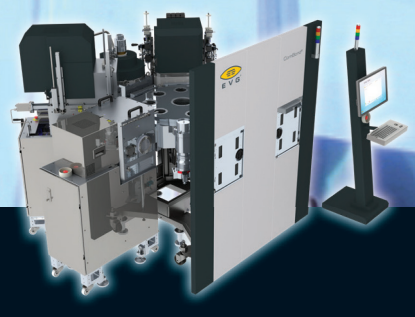

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In search of a **new solvent**

Although there is no universal successor to the widely used but increasingly outlawed solvent NMP, capable alternatives are coming to the fore

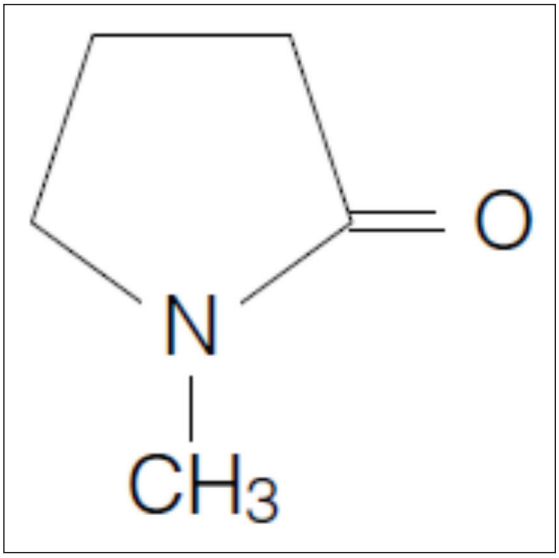
BY ANIL VIJAYENDRAN AND JOHN TADDEI FROM VEECO INSTRUMENTS

SOME OF THE MORE COMMON processes within the semiconductor manufacturing industry include positive photoresist stripping, developing and metal lift-off. For all these tasks, a very popular solvent is an organic compound with a five-member-ring that is known as NMP (or, to give it its full title, 1-methyl-2-pyrrolidone or 1-methyl-2-pyrrolidinone, N-methyl-2-pyrrolidone). NMP is effective in removing any photoresist residue while leaving the surface in good shape for downstream processing, and unlike some harsh solvents of the current era, it is not a carcinogen (although it is a reproductive hazard).

These advantages have helped NMP to become an industry standard, displacing a previous generation of solvents, thanks to superior chemical properties (see Table 1). Compared to a popular solvent of yesteryear, acetone, NMP has a far higher flashpoint – this allows processing below this temperature, improving safety.

In addition, NMP has a lower vapor pressure, leading to far lower emissions of volatile organic compounds, and recycling of this material can exceed 99 percent, even for pressurized dispenses. Yet another merit of NMP is that its photoresist saturation level is high,

NMP, which has the chemical formula C_5H_9NO and a molar mass of 99.1 g/mol, has been used for wide range of applications, thanks to its great characteristics that include: a high flash point compared to similar solvents; the capability to mix with water in all proportions; miscibility with most organic solvents; a high boiling point, a low freezing point and being relatively easy to handle; and its chemical and thermal stability.



permitting processing of many wafers with recycled chemistry.

Within the compound semiconductor industry, NMP has made a name for itself as the preferred solvent for metal lift-off (see *The merits of metal lift-off* for details). However, it's future could be short-lived. That's because companies are looking to meet growing environmental health and safety requirements by decreasing the use of more harmful chemical formulations in compound semiconductor manufacturing.

In fact, NMP has already been partially phased out in the EU, which has greater regulatory pressure than other regions around the world (see Table 1). Other countries are to be expected to follow this lead as worker exposure is a serious matter. Refinements to process tool design and selection can greatly reduce exposure for fab personnel, but avoiding the use of this particular solvent is clearly a more rigorous solution.

In practice, up until now the concerns over environmental health and safety have generally been addressed with engineering controls in tool and fab design, and through real-time chemical monitoring of the air within the fab, to ensure that workers don't get close to exposure limits. As well as a gradual shift away from manually operated equipment, there have been refinements to the airflow in wet process tools. Improvements include increased exhaust, multiple exhaust inlets, and the introduction of compartments within a tool, so particular chemistries can be segregated. In other words, worker exposure has been addressed by changing the tools performing the processes, rather than switching solvents.

Exploring alternatives

The use of NMP will not disappear overnight, as some established processes have been granted an exemption. However, many of the grandfather clauses are becoming increasingly difficult to extend, and there are already proposals in the US to restrict the use of NMP, following the lead taken by Europe.

Not everyone will lament the loss of NMP. This solvent – which is hygroscopic, so it picks up water from the air within the fab, affecting its pH – can corrode device metallisation. When deionised water is used directly to rinse the NMP from a patterned wafer, multi-metal stacks may suffer galvanic corrosion, detrimental to the wafer. One way to avert this is to carry out a preliminary rinse with isopropyl alcohol, but this increases emissions of volatile organic compounds and adds to solvent waste. So, in some fabs, alternative chemistries are used to process bump, pillar and redistribution layers.

One of the reasons why NMP will not be replaced overnight is that no-one has been able to identify an alternative chemical with all the desired attributes. The list of desired attributes for an alternative are extensive, as the replacement must be inexpensive, non-hazardous, non-volatile, fast acting, residue free, non-odorous, non-flammable, non-corrosive, and have a long life and a high saturation point for resist loading. Ideally, the new chemical that sports all these attributes would be supplied from an established chemical manufacturer, providing tremendous product support and a worldwide distribution network.

That's a wish list that is not going to be fulfilled. There is no chemical with all the desired attributes, so there is no single replacement. Instead, process owners have to select a chemistry that fulfils the critical attributes required for their process, while complying with the constraints from their protocols.

Chemical	Flashpoint	Flash Volatilization	Evaporation	Flammability	Reactivity	Recycle Effective
NMP	91°C	Minimal	Low	Combustible	Low	99+%
Acetone	-17°C	High	High	Highly Flammable	Moderate	<50%

Table 1. Comparison of NMP versus acetone as a chemical used for photoresist stripping, developing and metal lift-off.

Timing to Eliminate NMP			
Driver/Region	Europe	North America	Asia
Regulation	Now	On Horizon	Nebulous
New Materials	Now	Now	Now
Health	Limit Exposure	Limit Exposure	Limit Exposure
Environment	Developing	Developing	Developing

Table 2. The timing to eliminate NMP varies by region.

Coming to the aid of engineers within many compound semiconductor fabs is dimethyl sulfoxide (DMSO). It is compatible with existing wet process tool platforms; it can be used in a pure form; it is offered by a number of chemistry suppliers; and it can strip both positive and negative photoresist. In addition, it provides the main ingredient in many proprietary chemistry blends, and does not have not have the reproductive concerns of NMP.

Within the medical industry, DMSO is used to transport medicine through the skin and into the blood stream. That attribute is ideal for medical patches, but concerning for the semiconductor manufacturing industry. The danger is that when DMSO is used with harmful ingredients such as tetramethylammonium hydroxide (TMAH) – a commonly used base that is an autonomic nervous system toxin – it has the potential to transport this into a worker's bloodstream via skin contact. Due to this, the environmental health and safety departments of some fabs are reluctant to permit DMSO as a substitute for NMP. This stance is not consistent, though. The medical use of DMSO highlights the benign nature of the chemical in its pure form.

The future of NMP

Removing NMP from legacy processes does not tend to involve the elimination of solvent processing; solvent processing is entrenched in the semiconductor industry, because it has proven to be a robust approach within the fabs. What's needed is to identify another solvent that can replace NMP, and successfully perform the resist strip or metal lift-off process within the available toolsets.

At Veeco, we have developed the PSP WaferStorm platform, a toolset that can ease this transition. Our equipment is designed not only for NMP, but can handle a wide variety of other solvents. Often the process times are similar to those that are used for NMP, so throughputs and process flows are hardly changed. But in some cases the processes are quicker, benefitting our customers.

To identify the methods to provide the best process results, our scientists and process engineers continue to work with many leading materials companies to evaluate the impact of different chemistries and equipment. We work with industry materials providers and process owners to qualify alternatives to NMP for chip production. The materials providers that we work with include EMD Performance Materials, Technic, Intelligent Fluids and Versum Materials. Thanks to these relationships, we are able to offer our customers a complete toolset, chemical and process solution.

The material suppliers that we work with are making much progress in providing alternatives to NMP. For example, EMD has developed the AZ KWIK Strip and AZ Removers 880, 910 and 920; Technic has successfully displaced NMP with its TechniStrip P1331 and TechniStrip Micro D2; and Versum Materials has developed Dynastrip AP7880-T.

We will continue to evaluate candidates for replacing NMP at our demo lab in Horsham, Pennsylvania. Here, our efforts focus on developing processes and generating data. The insights that this provides help our customers to enjoy a smooth transition when implementing a new chemistry at their sites.

The merits of metal lift off

WITHIN the compound semiconductor manufacturing industry, the most common method for patterning metal layers is to sputter or evaporate metal over patterned resist, and then undertake a metal lift-off step. The metal lift-off process begins by depositing a sacrificial material, such as a photoresist, on the substrate. The sacrificial material is then patterned, before depositing a metal on top of the substrate. After this, the sacrificial material is removed through exposure to solvent soaking and spraying. This leaves behind just the material deposited directly on the substrate.

Engineers may turn to metal lift-off processes when they need to pattern materials, but they cannot use etching, as this would damage the underlying materials on the substrate. Rather than using the acid-based etchants, which typically etch the compound semiconductor at a faster rate than the films on top of it, metal lift-off employs solvent chemistries which are compatible with these substrates. Another merit of metal lift-off is that the equipment required for this process is far less expensive than that for dry etching.

Today, depending on the process requirements, metal lift-off processes are carried out in wet benches or single-wafer systems. If the user has more challenging material to lift off, or strict chemistry usage requirements, single-wafer approaches tend to be preferred.

Gallium oxide:
Laying the foundation for tomorrow's success

Supporting the emergence of ultra-wide bandgap power electronics is the fast, high-quality growth of gallium oxide layers

BY KEITH EVANS, GREGG DODSON, JACOB LEACH, HEATHER SPLAWN AND TAMARA STEPHENSON FROM KYMA TECHNOLOGIES

THERE IS GOOD REASON to have concerns over the future of our planet. Average global temperatures are undoubtedly rising, due to increases in carbon dioxide emissions, and this trend could continue as energy demand climbs.

Against this bleak backdrop, two rays of hope are the increases in energy generated by renewables, such as wind and solar, and the tremendous potential for the electric car. In both these cases, improvements are possible by increasing the efficiency of power electronics. Succeed on this front and more energy will be fed into the grid from renewables, by increasing the efficiency for stepping up and down voltages and converting them between their AC and DC forms; and there will be an increase in the efficiency with which the energy from the car battery is converted into a form that drives the wheels. The latter is a major plus point – it trims the automobile's running costs and boosts its driving range, gains that could lead to increased sales and ultimately better economies of scale.

Today, the majority of incumbent power devices are made from silicon. This enables low-cost manufacturing of diodes and transistors. However, silicon's intrinsic properties are overshadowed by those with a wider bandgap, notably SiC and GaN. These rivals have greater critical fields, primarily due to their larger bandgaps, and this allows them to excel in all the key figures-of-merit (FOM): Baliga's FOM, Baliga's high-frequency FOM, Johnson's FOM, and Keye's FOM. These higher FOM enable SiC and GaN devices to block higher voltages, more efficiently switch electrical current on and off, and more efficiently pass electrical current when the switch is in the on-state. Due to all these virtues, wide-bandgap materials offer energy-efficiency savings over silicon in all power electronics applications.

Recently, these devices have come a long way. Rewind the clock to the end of the previous decade, and nearly all of the SiC and GaN power electronics development was taking place in R&D labs. But in the intervening years this has changed dramatically, with devices reaching a state of maturity that has led to commercial traction, particularly for SiC.

Sales are accelerating due to the great gains in performance, such as a 90 percent reduction in efficiency losses during electric-power switching, which can take place during regenerative braking in hybrid and all-electric vehicles and in electric converters connecting wind farms to the grid. But that's not the only significant attribute of these wide bandgap power devices. Unlike those made from silicon, they don't need cooling to work well. In addition, they can be made smaller, to feature in circuits operating at higher switching frequencies that contain smaller passive components. The upshot is smaller, more efficient units that require less cooling and are more reliable and robust.

From wide to ultra-wide

These wide bandgap materials are taking the power electronics industry on a journey that may not stop with SiC and GaN, but continue onwards, to a class of materials known as ultra-wide bandgap semiconductors. These lesser-known materials, which

include AlN, AlGaN, Ga_2O_3, and diamond, promise to deliver further advances in the size, weight and efficiency of electrical units (see Figure 1 for a plot of unipolar electronic device figures-of-merit for silicon, GaAs, 4H-SiC, GaN, β-Ga_2O_3, AlN and diamond).

At Kyma Technologies of Raleigh, NC, we are developing an ever-expanding portfolio of technologies related to wide bandgap and ultra-wide bandgap materials. Our efforts include the development of crystal growth processes and tools for making these materials. We are routinely growing AlN, AlGaN, GaN, Ga_2O_3, and diamond materials; and we are routinely fabricating GaN devices.

Our current programme includes the development of Ga_2O_3 devices. We have mastered the growth of high-quality, *n*-doped films of Ga_2O_3 by HVPE, and our next challenge lies with device development.

If ultra-wide bandgap materials are to fulfil their potential, manufacture must involve large-area substrates, used to produce high-quality epiwafers at high growth rates. Large-area substrates are a pre-requisite to success, as they drive up manufacturing efficiencies and slash the cost of every device produced. It is for this reason that silicon technology has progressed from research on 1-inch wafers to production on initially 100 mm wafers, and then on to those with diameters of 150 mm, 200 mm and 300 mm. That's not the limit – 450 mm wafers exist today, but are yet to be used widely. When it comes to epitaxy, a key requirement for manufacturing vertical devices is the growth of thick, controllably doped *n*-type drift regions on large-area substrates. This has to be accomplished at the lowest possible cost of epitaxy per unit area. Due to all the reasons outlined above, when we develop our technologies, we make sure that they are compatible

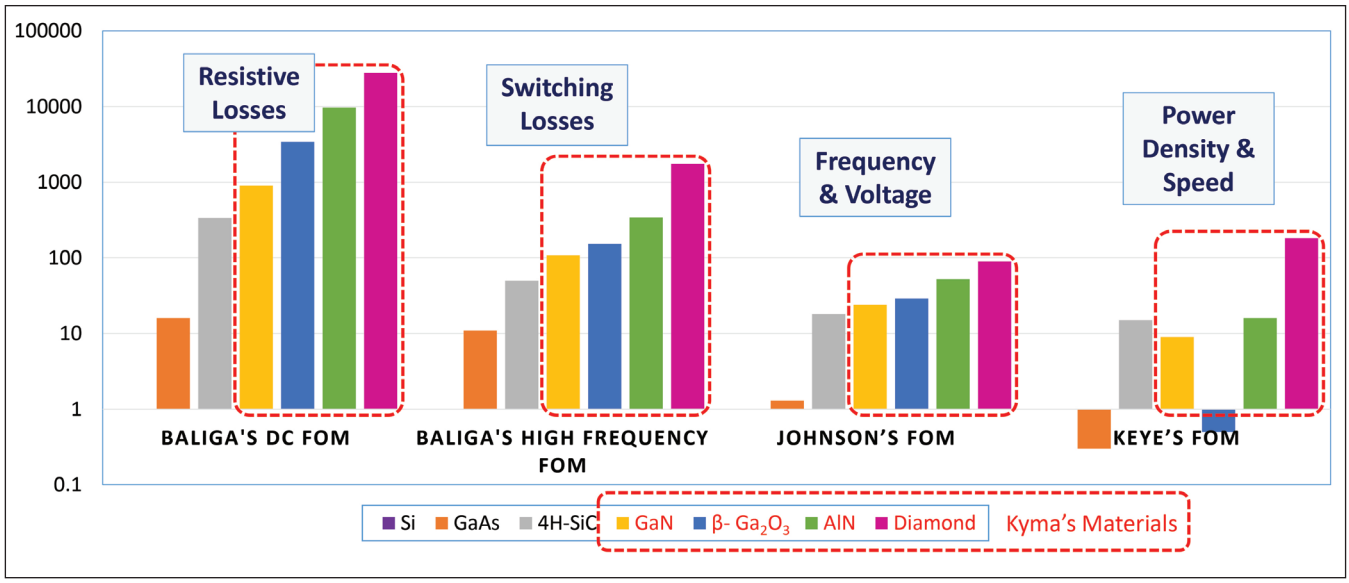


Figure 1. Four common unipolar electronic device figures-of-merit (FOM) for silicon, GaAs, 4H-SiC, GaN, β-Ga_2O_3, AlN, and diamond. Kyma's materials in development or for sale are identified by the red dashed lines.

with large-area materials and ensure high-purity, high-rate growth.

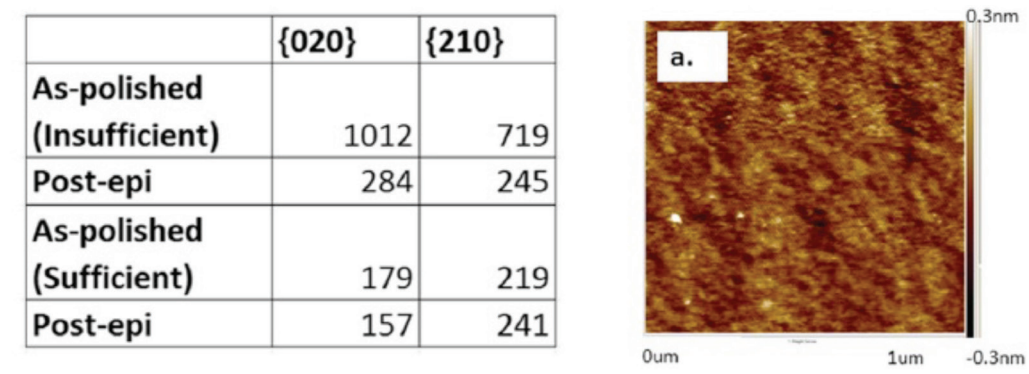
Our Ga_2O_3 products include β-Ga_2O_3 substrates, homoepitaxial β-Ga_2O_3 epiwafers, α-Ga_2O_3 epiwafers grown on sapphire substrates, and crystal growth tools for growing those epiwafers (see Figure 2 for an overview). Thanks to our vertically integrated approach, we can control the final finish of the substrate before engaging in epitaxial overgrowth. We offer this as a service too. Customers can supply us with their substrates, and even their grown epiwafers, and we can polish them. In addition, if desired, we can impart a defined mis-cut.

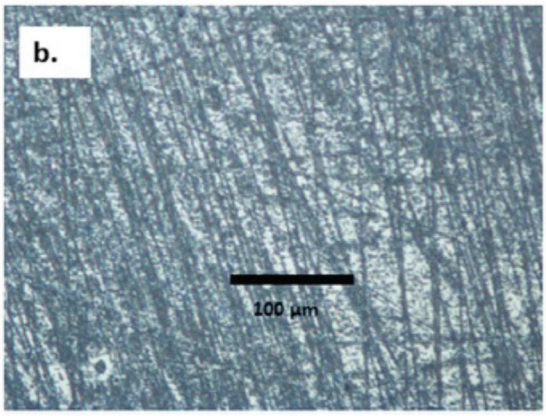
For more than 15 years, we have been using HVPE to grow GaN, AlN, and AlGaN materials. Back in late 2015 we decided to convert one of our GaN HVPE tools so that it could be used to grow homoepitaxial β-Ga_2O_3 epiwafers for a partner of ours that supplied the substrates.

Making the transition from growing GaN to Ga_2O_3 went against the grain. For many, many years, oxygen has been our enemy, but now it was needed to be more prevalent in the crystal than gallium, if we were to be successful. This transition posed many questions. Did we need to add a purified oxygen source to our tool, or would clean dry air suffice? How vulnerable

Figure 2. Kyma's Ga_2O_3 related products and services.

	{020}	{210}
As-polished (Insufficient)	1012	719
Post-epi	284	245
As-polished (Sufficient)	179	219
Post-epi	157	241





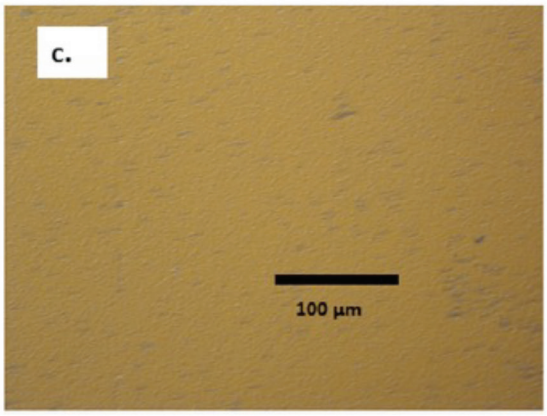


Figure 3. Table of X-ray diffraction arcsecond linewidths, defined as the full-width at half-maximum, for as-polished wafers and post-HVPE films using insufficiently polished and sufficiently polished processes. (a) 1 x 1 µm AFM image of a polished (010) β-Ga_2O_3 substrate and optical microscope images after 0.5 µm of homoepitaxial β-Ga_2O_3 growth using (b) an insufficiently polished and (c) a sufficiently polished substrate.

would our GaN-optimised tool be to the generation of particulates in the form Ga_xO_{1-x}? And would the high degree of chemical purity that is realised with our GaN growth process also lead us a high chemical purity in Ga_2O_3 growth capability?

Fortunately, we had help in answering all these questions. There is a wealth of information in the literature – we thank especially the incredible researchers in Japan for sharing their findings, by publishing their exciting results in all aspects of Ga_2O_3, including the application of HVPE technology. These insights have helped us to establish a HVPE process for producing high-quality homoepitaxial β-Ga_2O_3 and heteroepitaxial α-Ga_2O_3 films at growth rates ranging from 2 µm/hr to 20 µm/hr.

We have found that when growing β-Ga_2O_3 films by HVPE, getting the right substrate preparation and offcut angle is critical to getting a good surface morphology and a high-quality epilayer. It is difficult to detect sub-surface damage on a freshly prepared β-Ga_2O_3 substrate, but any imperfections that are there give rise to morphology issues during HVPE overgrowth of β-Ga_2O_3.

Compromised material quality is evident in the linewidths of X-ray diffraction scans (see the table in Figure 3). These results have helped us to improve our polishing process, so that it is capable of adequately removing sub-surface damage. The result is a relatively flat surface, according to atomic force

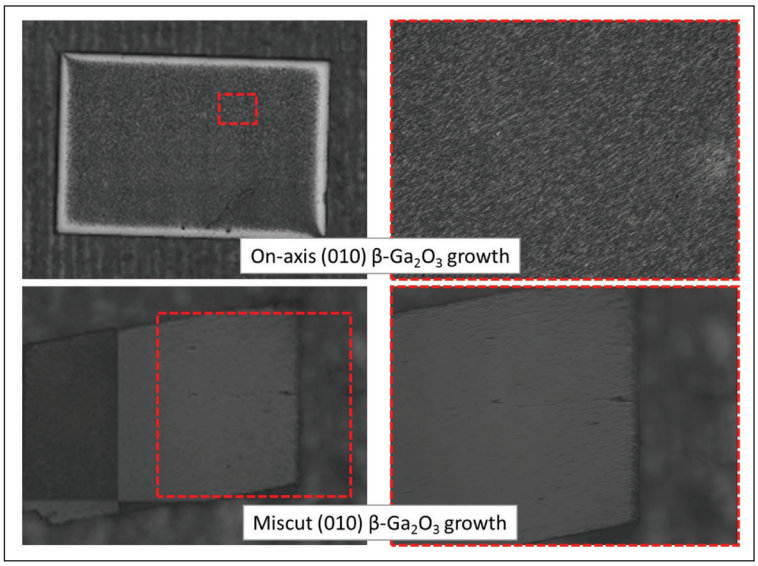


Figure 4. Optical microscopy images of β-Ga_2O_3 films obtained using the nSPEC artificial-intelligence-enabled, rapid-inspection tool that Kyma brought in-house in 2013. This tool serves as a workhorse, used by Kyma to measure almost every epiwafer or substrate made, and to scrutinise many incoming materials prior to use. Lower magnification images on the left and higher magnification images on the right show a much smoother film morphology for homoepitaxial β-Ga_2O_3 growth on properly mis-cut substrates (bottom), when compared with growth on on-axis substrates (top).

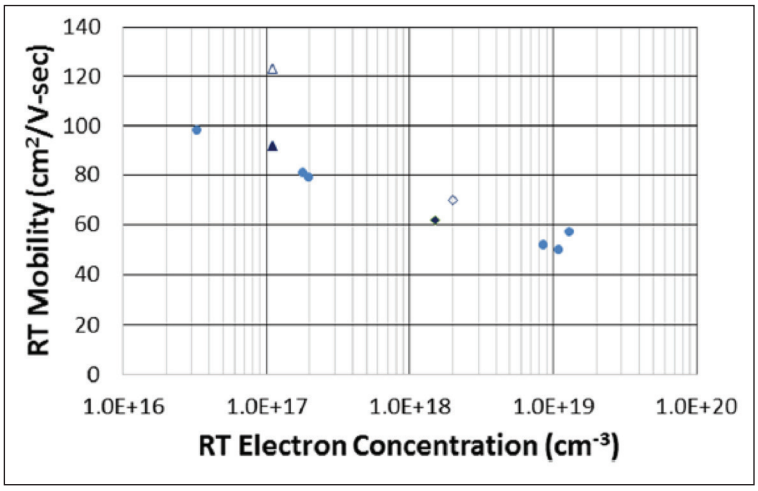


Figure 5. Room temperature mobilities vary with electron concentration in films grown on bulk β-Ga_2O_3. Triangles and diamonds represent films grown under identical conditions, except that the diamonds represent intentionally silicon-doped films, while the triangles represent unintentionally doped films. The open triangle and open diamond represent growths on bulk substrates with higher structural quality – these epilayers exhibit linewidths of less than 100 arc sec for {020} reflections.

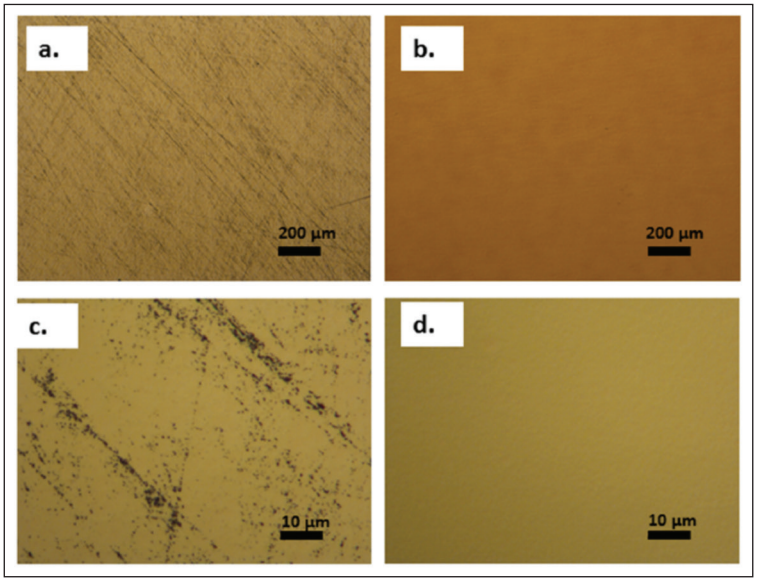


Figure 6. Microscope images of 1 µm-thick films of α-Ga_2O_3 at: 20x, for (a) and (b); and 100x, for (c) and (d). The film grown on the properly polished substrate, imaged in (b) and (d), has a far better surface morphology than that shown in (a) and (c), images of the film grown on the unsuitably polished substrate.

microscopy (see Figure 3(a)), and a far better surface after HVPE growth of β-Ga_2O_3 films (compare the optical microscopy images in Figure 3 (b) and (c)).

Optical microscopy also highlights the influence of the surface off-cut on the epilayer surface morphology. We have used this technique to compare the surface morphology of two homoepitaxial β-Ga_2O_3 films grown under identical growth conditions at 1000 °C. The pair of substrates we have used are nominally identical bulk (010), but one is on-axis and the other mis-cut by about 2° in a preferred direction. Images, collected by a rapid-inspection tool provided from Nanotronics that is equipped with nSPEC artificial intelligence, clearly show that a mis-cut substrate results in superior surface morphology (see Figure 4).

Having addressed optimisation of the surface mis-cut, eliminated sub-surface damage, and optimised the growth chemistry, we have gone on to produce a range of *n*-type homoepitaxial β-Ga_2O_3 films with differing electron concentrations. Assessing them with Hall effect measurements reveals that as electron concentration falls from around 10^{19} cm^{-3} to 10^{17} cm^{-3}, mobility decreases from around 90 to 120 cm^2 V^{-1} s^{-1} to around 50 to 60 cm^2 V^{-1} s^{-1}. Grow rates are controllable, for the range 2 to 20 µm/hr.

We have also investigated the growth of films of α-Ga_2O_3. Compared to its thermodynamically stable sibling β-Ga_2O_3, this polytype is metastable, has a higher crystalline symmetry and sports a wider bandgap, making it an interesting choice for device applications. It major weakness is that it cannot be grown from the melt, so films of α-Ga_2O_3 have to be grown on a non-native substrate.

Sapphire is the obvious choice, given that α-Al_2O_3 is the thermodynamically favoured form of crystalline Al_2O_3, and that it is possible to grow α-Ga_2O_3 on α-Al_2O_3. As is the case with homoepitaxial β-Ga_2O_3 films, surface preparation is essential for growing high-quality films. Evidence from optical microscopy highlights this requirement, clearly exposing the difference in morphology between α-Ga_2O_3 grown on *c*-plane sapphire substrates that have been properly and improperly polished (see Figure 6). Optimise the substrate's surface, and it's possible to realise excellent surface morphology.

We have made significant strides with Ga_2O_3. We're pretty excited that we now have good control over substrate preparation, growth chemistry, *n*-type doping, surface morphology, and background doping. These capabilities are going to lay the foundations for our move to device development. We believe that of the two polytypes of gallium oxide, it is β-Ga_2O_3 that has the greatest potential to gain commercial acceptance, especially in high-voltage power switching. Yet because β-Ga_2O_3 on α-Al_2O_3 has the advantage of a more mature substrate supply chain, we'll remain active in that approach as long as our customers support it. We hope to play a role in bringing each of these technologies to market over the next few years.

Further reading

J.H. Leach *et al*. APL Mater. **7** 022504 (2019)

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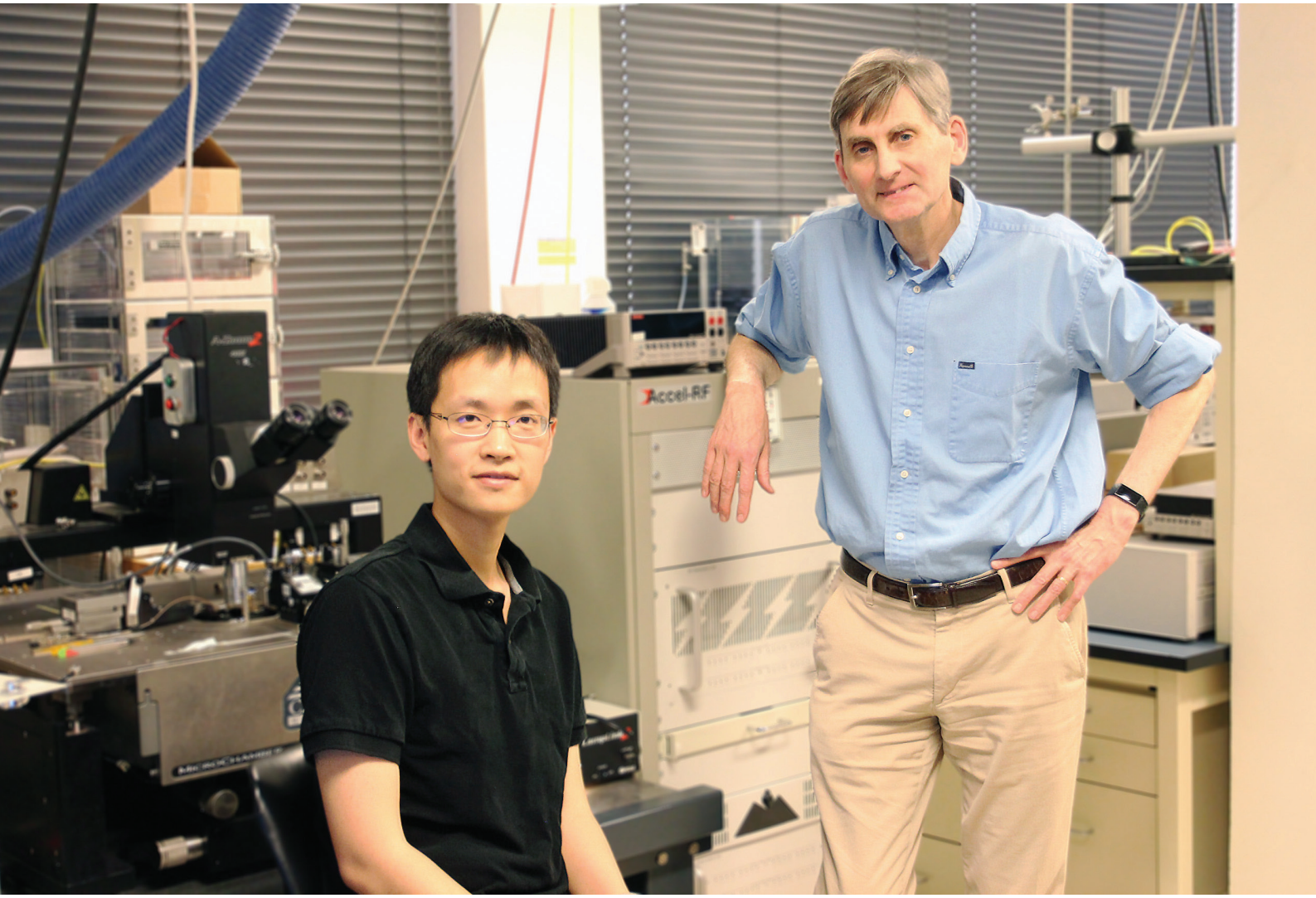

Novel etching technique yields the smallest InGaAs FinFETs

Thermal atomic layer etching produces incredibly small InGaAs FinFETs with record-breaking performance

BY WENJIE LU, YOUNGHEE LEE, JESÚS DEL ALAMO, AND STEVEN GEORGE FROM MASSACHUSETTS INSTITUTE OF TECHNOLOGY AND UNIVERSITY OF COLORADO BOULDER

FOR THE PAST FIVE DECADES, the microelectronics revolution has been driven by the scaling of silicon CMOS. Reducing device dimensions has delivered continuous improvements in transistor performance, enabling this device to faithfully follow Moore's law. The question is, how much longer can this go on?

Throughout the twentieth century, advances in CMOS technology came from shrinking the dimensions of the planar transistor. But recently the design of the device has had to change. Modifications include the introduction of three-dimensional architectures that create severe production challenges, which must be overcome when manufacturing state-of-the-art silicon multi-gate transistors, such as the latest FinFETs. This class of transistor has already reached the sub-10 nm regime – for example, the latest Intel 10 nm FinFETs

feature fins that are merely 7 nm wide.

Such miniaturisation is an extraordinary feat of human engineering, unthinkable even a decade ago. And it's not just a matter of simply reducing the width of the FinFET – this must go hand-in-hand with a fin that is tall enough to support a high current density. Do this, and you can fulfil performance criteria, but you'll have a very fragile structure.

Another characteristic of the modern FinFET is a performance that is dominated by its surface area. So, to ensure that it work wells, it has to have a high-quality MOS interface. This requirement, which is retained as scaling continues, has to be realised with etching technologies that support sub-nanometre precision and fidelity, while yielding highly perfect interfaces. This is out of reach for today's mainstream etching methods.

Thermal atomic layer etching

In silicon fabs, the most common method for patterning micro and nano-scale structures is plasma etching. In use since the 1970s, this essential step of CMOS fabrication has evolved, becoming ever-more sophisticated. However, it can only go so far. New forms of etching are now needed that are more benign and versatile, while providing sub-monolayer etch control, so that fabs can produce sub-10 nm, 3D structures.

Recently, a new class of etching has been attracting much attention. Known as atomic layer etching, or simply ALE, it is the most advanced etching technique today. It is essentially the reverse of atomic layer deposition (ALD), based on two self-limiting steps: the modification of the device surface by a reactive species; and then the selective etching of the modified surface, to leave an untouched substrate beneath.

ALE can be sub-divided into two types. The more common, known as plasma ALE, has realised tremendous progress in the last few years, and involves the modification of the surface by a reactive plasma, such as Cl_2 plasma. Etching follows by introducing energetic ions or neutrals, such as an argon plasma, into the chamber. With this technique, etching is anisotropic – that is, directional – a useful attribute for many processes that involve pattern transfer.

The other form is thermal ALE. It avoids a plasma, instead removing material through a chemical ligand-exchange process. The reaction sequence closely resembles that of atomic layer deposition, in which pulses of chemical precursors are introduced into a reactor to complete two individual self-limiting steps. Mirroring ALD, thermal ALE is an isotropic process. Thermal ALE is much younger than plasma ALE, having been first demonstrated in 2015, when it was used to etch an Al_2O_3 thin film. Since then, most reports on this technology have been limited to etching dielectric, metal and nitride thin films. There have been no device-level demonstrations.

Removing III-Vs

Our MIT-University of Colorado collaboration is addressing that omission, using the thermal ALE process to fabricate transistors. Efforts were initially directed at developing a thermal ALE technique for III-V compound semiconductors, and in particular InGaAs.

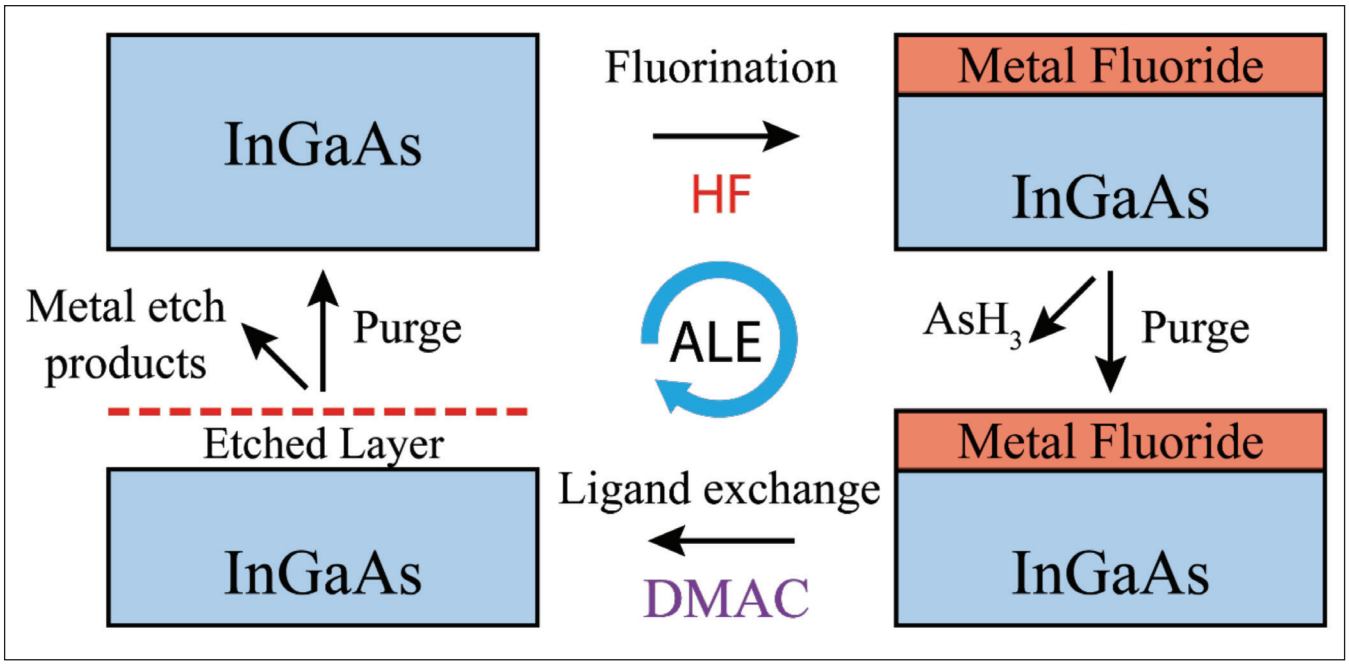

Figure 1. Schematic of a complete cycle of InGaAs thermal atomic layer etching. In the first half-cycle, the InGaAs surface is fluorinated, and metal fluorides are formed. In the second half-cycle, the metal fluorides are removed through a ligand-exchange process. The volatile etch products formed during each half-cycle are purged away.

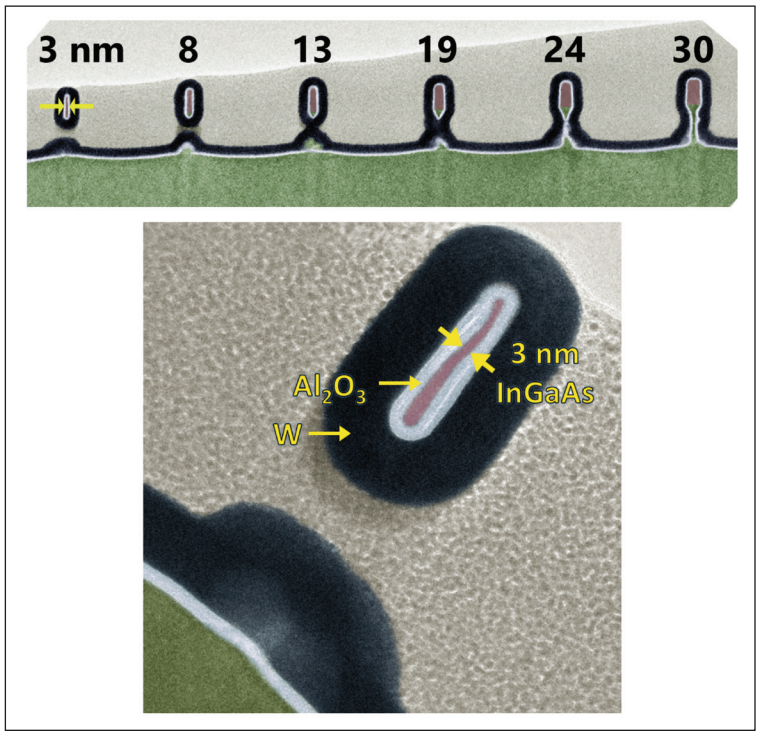

Figure 2. Cross-sectional transmission electron microscopy image of (top) InGaAs fins (fin widths of 3 nm to 30 nm) fabricated by the *in situ* ALE-ALD process, and (bottom) the smallest InGaAs suspended fin with a 3 nm fin width.

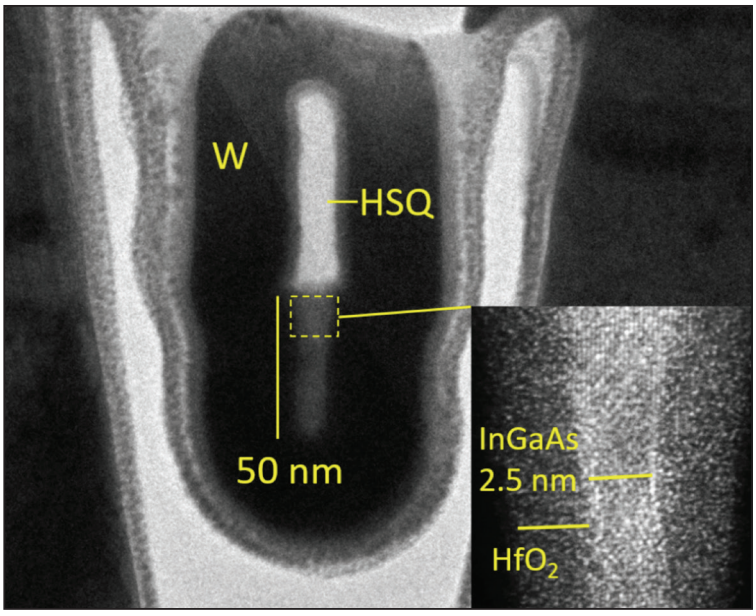

Figure 3. A cross-sectional transmission electron microscopy image of the most aggressively scaled InGaAs FinFET with fin width of 2.5 nm. Inset: close-up image of the upper portion of the fin channel.

We have focused on this ternary, because it is a promising material for CMOS logic and RF applications. Its merits include a very high electron velocity, which is the key to achieving a high performance at a lower operating voltage than the traditional silicon MOSFETs. Recently, rapid progress is being made with this type of device, including our demonstration, in 2017, of an InGaAs FinFET with a fin width down to 7 nm.

However, until our very latest work, carried out within the last year or so, the performance of the best InGaAs FinFETs was still at some distance from its true potential, primarily due to a poor MOS interface quality.

Before we delve into the details of our work, we wish to point out that the introduction of ALD had a dramatic impact on the performance of III-V transistors. Just over ten years ago, this deposition technique made its introduction into III-V MOSFET processing. Due to its self-cleaning effect, it was instrumental in mitigating surface Fermi-level pinning at the oxide-semiconductor interface.

Since then, the performance of the InGaAs MOSFET has skyrocketed. However, issues remain. Fabricating FinFETs requires aggressive plasma etching of channel sidewalls, and this is probably to blame for compromised electron transport. We are aiming to address this with thermal ALE.

After some experimentation, we have developed a working thermal ALE process for III-Vs. The first half-cycle is a surface fluorination step, using gaseous hydrofluoric acid, and the second half is a ligand-exchange process, removing metal fluorides on the surface (see Figure 1 for an outline of the sequence). By using dimethylaluminum chloride to remove the metal fluorides, we have a process that has all the etch products volatile at 300 °C, allowing them to be removed by purging. If we need to increase the depth of the etch, we simply repeat the cycle.

Trials at 300°C have determined etch rates of 0.2 Å/cycle and 0.6 Å/cycle, respectively, for InGaAs and InAlAs. In comparison, conventional self-limiting etching methods, such as digital etch, typically etch at a rate of the order of 1 nm/cycle, indicating that InGaAs thermal ALE is around fifty times slower. That's not an issue but a blessing, as when this technology is used for deep nano-scale device fabrication, it provides unprecedented etching control and precision.

What is even more exciting is that the similarities between ALE and ALD allow us to pair them together in the same reactor. This has enabled us to perform *in situ* ALE-ALD, an ideal process for forming the MOS gate stack in a FinFET. We gently etch into the fin sidewalls, in a plasma-free, isotropic fashion, using thermal ALE, before we switch to ALD to cover them with gate dielectric and metal.

This approach is very promising. It completely prevents air exposure to the MOS interface, and it offers much freedom – after we have decided which precursors to introduce into the reactor, we can freely switch between etching and deposition. Due to these strengths, plus the great level of control, this process offers new ways to undertake nano-scale device fabrication that should help to significantly improve transistor performance.

To highlight the capability of twinning ALE and ALD, we have used these two technologies to fabricate a series of InGaAs-Al_2O_3-W gate-all-around fin structures. These devices, formed with an *in situ* ALE-ALD process, feature InGaAs fins with widths ranging from 30 nm down to just 3 nm (see Figure 2). We have found that when the fin width is below 20 nm, the InGaAs channel is completely suspended, due to the ALE selectivity between InGaAs and InAlAs. The *in situ* process also produces a remarkably sharp interface between the InGaAs and Al_2O_3 layers. This gave us great hope when we embarked on creating the first transistor by thermal ALE.

Miniaturised FinFETs

Using our *in situ* thermal ALE-ALD technique, we have fabricated InGaAs FinFETs with a fin width from 18 nm to 2.5 nm and a fin height of 50 nm (see Figure 3 for transmission electron microscopy cross-sections of these transistors). The key to making these devices, which include the most aggressively scaled III-V FinFET to date, is the extremely low etching rate of thermal ALE. Note that the FinFET features an HSQ hardmask, used for fin reactive-ion etching, that is left in the finished transistor, and a gate stack consisting of 3 nm of HfO_2 and 30 nm of tungsten. The minimum gate length is 60 nm.

The merits of *in situ* ALE are not limited to the fabrication of extremely small devices, but extend to significant improvements in performance that result from the lack of exposure of the critical oxide-semiconductor interface to air, as occurs in common fabrication processes. Measurements on our InGaAs FinFETs show well-behaved transistor behaviour, even for the 2.5 nm-wide fins (see Figure 4). For these transistors, in the linear and saturation regime, subthreshold swings are just 62 and 68 mV/decade,

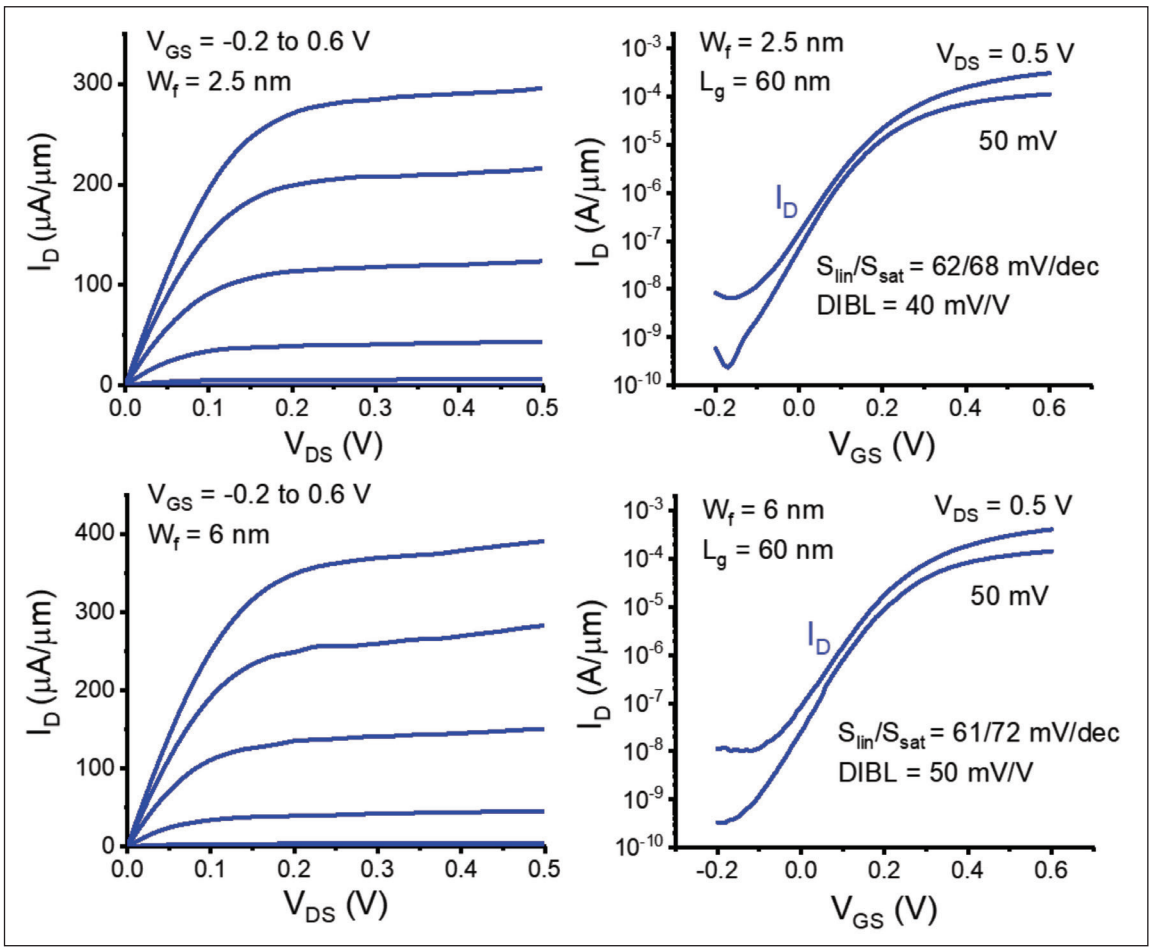

Figure 4. Output and subthreshold characteristics of InGaAs FinFETs fabricated by an in situ thermal ALE-ALD process. The FinFETs have a gate length of 60 nm, and a fin width of 2.5 nm (top row) and 6 nm (bottom row). All figures of merit are normalised by the conducting gate periphery.

respectively. These near ideal values, highlighting the capability of these devices to sharply turn-off, stem from the high quality of the MOS interface.

We have found that differences in fin width lead to changes in the maximum value for transconductance, a measure of the transistor's turn-on behaviour. Operating at a drain-source voltage of 0.5 V, the maximum transconductance is 0.85 mS/μm for a 2.5 nm fin, and increases to 1.2 mS/μm for a device with a 6 nm fin – the latter exhibits excellent electrostatic behaviour. For all devices, off-state current is limited by gate leakage.

To evaluate the benefit of our *in situ* process, we have compared the characteristics of our latest FinFETs with our previous generation of InGaAs FinFETs. Both sets of transistor have the same device design, and aside from the new thermal ALE process, they are fabricated in the same way.

Plotting the maximum transconductance and subthreshold swing as a function of fin width shows that the two types of FinFETs have a similar scaling behaviour (see Figure 5). In addition, they reveal that the thermal ALE process produces a 60 percent overall improvement in transconductance and a reduction in saturation subthreshold swing. For the new InGaAs FinFETs, the average subthreshold swings is 70 and 74 mV/dec in the linear and saturation regime, respectively. In comparison, the previous generation of devices have sub-threshold swings that are just below 100 mV for 5 nm fins, and nearly double this for 25 nm fins. This deterioration in sub-threshold swing with wider fins is minimal in devices made with the *in situ* ALE/ALD process.

We have also observed a consistent reduction in drain-induced barrier lowering with our *in situ* ALE/ALD process. This finding, and the values for the maximum transconductance and subthreshold swing, underline the extraordinary enhancement in electrostatic control that results from the superior MOS interface quality obtained by the *in situ* thermal ALE-ALD process.

To evaluate the performance of our latest InGaAs FinFETs, we have benchmarked their peak transconductance against other state-of-the-art InGaAs FinFETs. Our survey of the literature reveals a record peak transconductance for all our III-V FinFETs with fin widths below 20 nm.

We have also compared our devices with commercial silicon FinFETs. For a 7 nm fin width, which corresponds to the 14 nm and 10 nm nodes, our InGaAs FinFETs match the performance of Intel's 14 nm node FinFETs. This is a great result, considering our device's lower operating voltage – V_{DD} is 0.5 V for InGaAs and 0.7 V for silicon – and our longer gate length.

Our results are extremely encouraging, given that these transistors are the first to be made by thermal ALE. They clearly show great promise, while highlighting potential for thermal ALE, which could lead to improvements in other nano-electronic devices. This technique is truly versatile: it can be applied to a wide range of materials and device structures, such as vertical nanowires; and it offers engineers new opportunities to design and fabricate devices at the atomic level. As Feynman would say, "There's plenty of room at the bottom!"

Further reading

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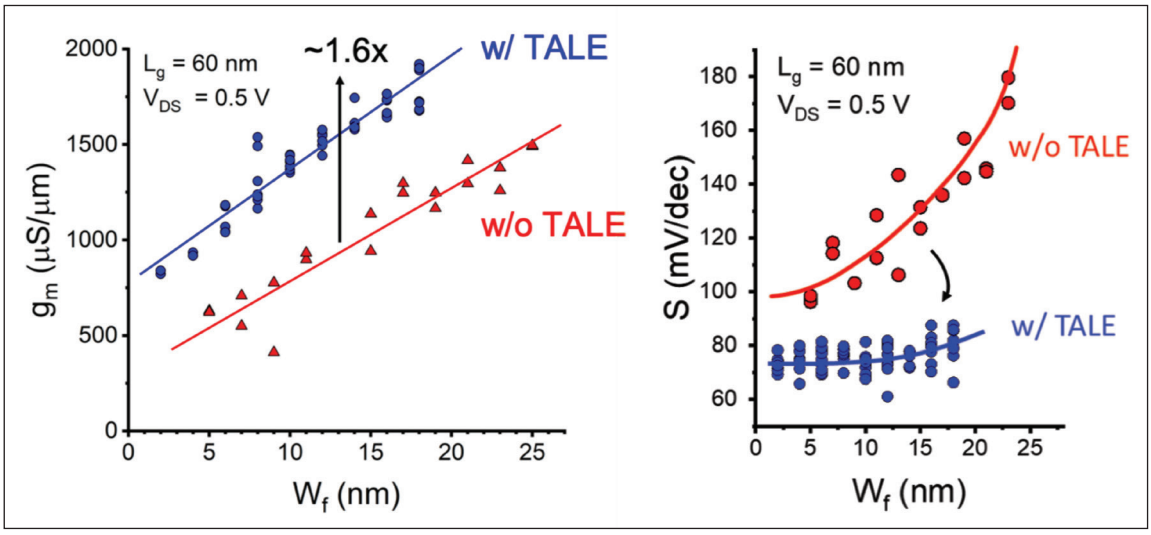


Figure 5. Scaling behaviour of (left) transconductance and (right) subthreshold swing versus fin width of InGaAs FinFETs at V_{DS} = 0.5 V, with and without the *in situ* thermal ALE-ALD process. All FinFETs have a gate length of 60 nm.

Cutting the cost of III-V cells

HVPE speeds the growth of InGaP cells and trims their cost

ALTHOUGH the efficiency of III-Vs cells trumps those of other technologies, their deployment is held back by high costs, which are associated with substrates and epitaxial processes.

But their epitaxial costs don't have to be so high, according to work by a team from Japan. The solution: turn to HVPE.

The researchers, from the National Institute of Advanced Science and Technology (AIST) and Taiyo Nippon Sanso Corporation, have used HVPE to form an InGaP cell. Created with growth rates of tens of microns per hour, this single-junction device has a peak external quantum efficiency of well over 60 percent.

The long-term goal for the team is to combine this HVPE-grown cell with those made from dissimilar materials, using their bonding technique known as smart stack.

"Our aim is to realise low-cost hybrid multi-junction solar cells with high efficiencies, such as III-Vs and silicon, and III-Vs and CIGS," says AIST's Yasushi Shoji.

HVPE is cheaper than the most common approach used for growing III-V cells, MOCVD, because it uses a pure metal rather than a metal organic precursor, which is about an order of magnitude more expensive. A pure metal source is also used in MBE, but the growth rates for this technology are only around a micron per hour, hampering throughput and escalating cost.

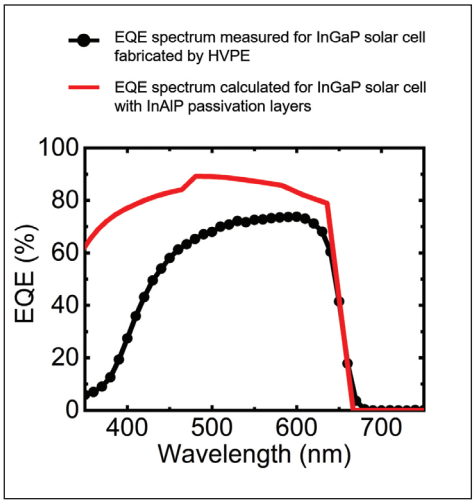
The team from Japan grow their cell in a vertical-flow-type H260 HVPE tool made by Taiyo Nippon Sanso. It features two growth chambers. "Multi-growth chambers are needed to form abrupt interfaces," explains Shoji.

After loading *p*-type (100) GaAs substrates with a 4° mis-cut into the reactor, the engineers grow a *p*-type GaAs buffer layer, followed by a 230 nm-thick layer of *p*-type InGaP, an 800 nm-thick layer of lower doped *p*-type InGaP, a 200 nm-thick layer of *n*-type InGaP, and finally an *n*-type GaAs contact layer. The composition of the InGaAs layers are chosen to ensure lattice-matching to GaAs.

Completion of the single-junction cell involves the addition of *p*-type and *n*-type ohmic electrodes, followed by the removal of the top *n*-type GaAs contact layer, and the addition of an anti-reflection coating.

Initially, two variants of the cell were produced by the team: one with InGaP grown at 660 °C, using a growth rate of 14 μm/hr; and the other with InGaP grown at 680 °C, using a growth rate of 20 μm/hr. Lowering the temperature led to a hike in the short-circuit current density from 1.4 mA cm^{-2} to 10.7 mA cm^{-2}, an increase in the open-circuit voltage from 1.15 V to 1.31 V, a gain in fill factor from 0.76 to 0.84, and a leap in efficiency – it rocketed from 1.3 percent to 11.8 percent.

X-ray diffraction reveals the reason behind all these gains in performance. During growth at 680 °C decomposition took place in the InGaP layer, to form regions with indium compositions of 48 percent and 41 percent. Lowering the growth temperature by 20 °C resulted in a uniform film.



HVPE enables high-quality cells to be produced using InGaP growth rates of 40 μm/hr.

Having established the appropriate growth temperature, the researchers produced InGaP films at growth rates up to 54 μm/hr, which is about ten times higher than that associated with MOCVD.

In the work reported in the paper, cells were not fabricated from material produced with an InGaP growth rate of 54 μm/hr. "The carrier concentration was too high for cell structures," says Shoji. Recently, however, the researchers have improved their growth system. This enables even higher growth rates, and the fabrication of cells from material formed with InGaP growth rates of 54 μm/hr.

Cells formed with a InGaP growth rate of 40 μm/hr had an external quantum efficiency of over 60 percent. That's by no means the limit, though, with calculations suggesting that if an InAlP passivation layer is added, efficiency could increase to over 80 percent.

Shoji and co-workers are now trying to improve the efficiency of their cells, which will require the growth of aluminium-containing layers by HVPE.

Reference

Y. Shoji *et al*. Appl. Phys. Express **12** 052004 (2019)

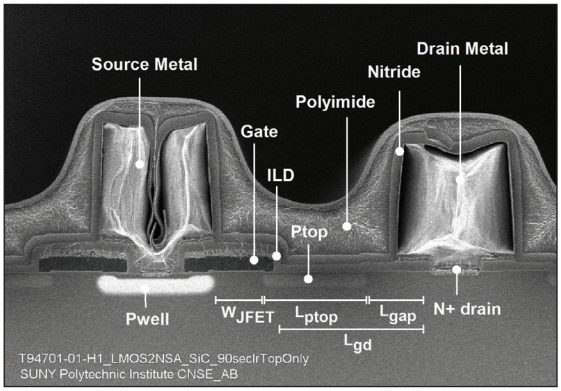
SiC: Towards the integrated circuit

SiC integrated circuits are one step closer to realisation, thanks to the development of lateral MOSFETs with record-breaking currents

WITH SiC diodes and transistors now well-established products, the next big challenge is the SiC IC. This will enable many applications that require a wide range of voltage and power ratings, such as automotive, industrial and electronic data processing, energy harvesting and power conditioning.

Making much headway towards this goal is a team from the State University of New York Polytechnic Institute, Albany. These researchers claim that they have recently broken new ground by propelling the current handling performance of a key building block for the SiC IC, the high-voltage SiC lateral MOSFET, from a few milliamps to 10 A.

Spokesman for the team, Nick Yun, says that during development of the 600 V device, he and his co-workers focused on innovation of the design, and using mature processing technology found in a production-grade fabrication facility. The MOSFETs were made at X-Fab, a 6-inch wafer foundry in Texas.



A scanning electron microscopy cross-section of the lateral SiC MOSFET. The critical dimensions, which are labelled, are: the width of the JFET, W_{JFET}; the length of the *p*-type top region, L_{ptop}; the gap between the *p*-top and the *n*-type drain, L_{gap}; and the gate to drain distance, L_{gd}.

According to Yun, one of the most important aspects of the work is the discovery that in these lateral devices, the drift-layer resistance is a relatively small contributor to overall resistance.

"Instead resistances from the metal contact and the channel account for the largest portion," says Yun.

Fabrication of the device began by forming a 6 μm-thick *n*-type drift layer, before the addition of aluminium and nitrogen implants defined *p*-type and *n*-type regions. They included a lightly doped *p*-type region that reduces the surface electric field near the main junction. This lightly doped structure sits above a *p*-type well, and must be carefully placed, because it defines the JFET width along the *p*-type well region.

Additional critical dimensions within the lateral MOSFET include the length of the *p*-type top region, and its gap to the *n*-type drain. They must be chosen to ensure that breakdown occurs at the drain junction, rather than at the surface or the gate oxide. Note that the specific on-resistance is proportional to the length of the *p*-type top region, so it cannot be too wide.

To activate the implanted ions, the wafer is annealed at 1650 °C for ten minutes. Dry oxidation at 1175 °C adds a 50 nm-thick gate oxide, before deposition and patterning of a poly silicon gate follows, and then the addition of a interlayer dielectric. Subsequent etching opens up ohmic contact regions, with metals added to form the source and drain contacts and a gate pad, before the front-side of the wafer is passivated by nitride and polyimide.

The team extracted resistance components for their lateral MOSFETs from current-voltage measurements, conducted between 0 V to 30 V in 5 V steps, at two temperatures: 25 °C and 150 °C.

They found that at room temperature the biggest contributions to the resistance came from the channel and the contact – together they accounted for 34 percent of the total. Other components – such as resistance associated with accumulation, the JFET region and the drift – only accounted for 8 percent. The lion's share, 57 percent, is attributed to "others", and is predominantly the metal resistance from the interdigitated fingers.

At 150 °C, the channel and contact were still the leading contributors to resistance, but that associated with the JFET had climbed from 3 percent to 11 percent. This is due to a reduction in bulk mobility.

Yun and co-workers point out that they could reduce the on-resistance by increasing channel mobility. In the device it is 17 $cm^2 V^{-1} s^{-1}$, and if it were increased to 30 $cm^2 V^{-1} s^{-1}$, this would trim the channel resistance from 3.5 $m\Omega\ cm^2$ to 1.9 $m\Omega\ cm^2$, reducing its contribution to the total resistance from 25 percent to 14 percent.

The team will now focus on optimising its lateral MOSFET. "We shall pursue various corrective actions, such as modification of the chip layout to reduce the resistance from metal routing, improved metal contact formation technology, evaluation of packaged devices, and use of different substrates," says Yun.

Reference

N. Yun *et al*. Appl. Phys. Lett. **114** 192104 (2019)

SiN: A panacea for current collapse

A SiN passivation layer even combats current collapse in ultra-wide bandgap GaN HEMTs

CURRENT COLLAPSE impairs the performance of III-N HEMTs. It degrades their microwave output and increases the dynamic on-resistance of power switches.

This malady is so significant that it has been extensively studied in conventional GaN-based HEMTs, which have AlGaN channels with a low aluminium content. And now, thanks to efforts at the University of Carolina, it has been investigated in ultra-wide bandgap HEMTs, sporting $Al_{0.4}Ga_{0.6}N$ channels. In these transistors, the remedy is the same as that for conventional HEMTs – passivation with Si_3N_4.

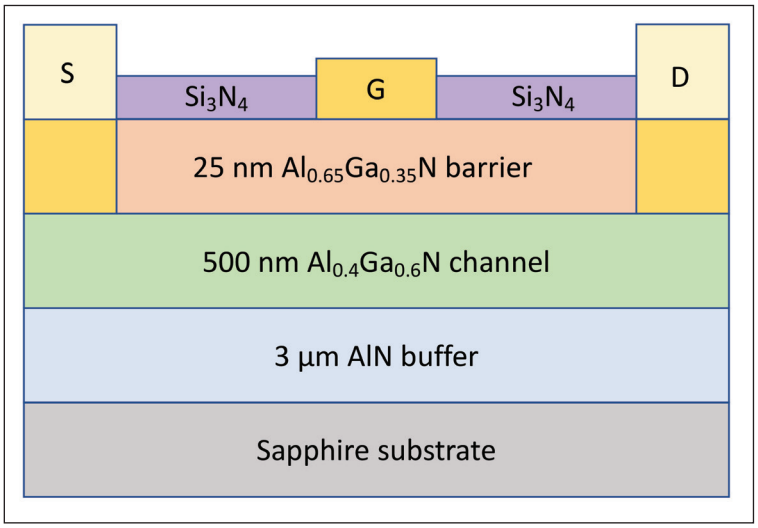
The team came to this conclusion after comparing the performance of passivated and unpassivated HEMTs. They were produced by taking an AlN-on-sapphire template with a 3 mm-thick AlN buffer layer that has a defect density of about 1-3 x 10^8 cm^{-2} and adding, by MOCVD, a 500 nm-thick $Al_{0.4}Ga_{0.6}N$ channel and a 30 nm-thick, silicon-doped $Al_{0.65}Ga_{0.35}N$ barrier layer. Using the Eddy current method, capacitance-voltage measurements indicate that this structure has a two-dimensional electron-gas sheet density of 1.9 x 10^{13} cm^{-2}.

Etching into the barrier with a chlorine-based inductively coupled plasma, and subsequent electron-beam deposition of a metal stack created source and drain contacts. Thermal annealing for 30 seconds at 950 °C under nitrogen gas enabled a contact resistance for the source and drain of just 1.64 Ω cm. Gates were then added, before passivated devices were formed with the addition of a 300 nm-thick Si_3N_4 layer by plasma-enhanced CVD.

Current-voltage characteristics were determined for both static and dynamic conditions. The latter involved pulses with a duty cycle of 100 and a length that varied from 500 ns to 1 ms.

Measurements on devices with a 1.8 μm-long gate and a 6 μm source-drain spacing showed that the unpassivated devices suffer from significant current collapse when driven with pulses. Passivated devices with the same dimensions are free from this affliction.

For the unpassivated devices, the degree of current collapse diminishes as the pulse width lengthens from 100 ns to 1 ms. This results from an increase in the time that the device is in the on-state and can undergo electron de-trapping. By varying the length of the pulses, the researchers were able to discover that the time taken for electron emission from the traps is in the range 1 μs to 1 ms – and that the most common emission time is about 200 μs. The latter figure corresponds to an emission rate of 5 x 10^3 s^{-1}, which is two-to-three orders of magnitude lower than that for conventional HEMTs, due to the higher bandgap.



Depositing a SiN passivation layer by plasma-enhanced MOCVD slashes current-collapse in ultra-wide bandgap HEMTs.

To determine which region of the device is responsible for current collapse, the team turned to measurements based on the gated transmission line model. Plots of resistance as a function of gate length were made for measurements on HEMTs with gate-source and gate-drain openings of 10 μm, and gate lengths varying from 10 μm to 100 μm.

These measurements revealed that the primary contributor to the current collapse is the access region resistance. In addition, they showed that electron trapping has very little impact on the channel resistance under the gate.

Based on these measurements, the team identified the cause of current collapse as either carrier trapping in the access region, strain modulation in the access region, or a combination of these two.

"We are conducting more detailed studies to determine the exact dominant mechanism of current collapse in these new devices, and the results will be published when available," wrote the team in their paper.

Reference

S. Mollah *et al*. Appl. Phys. Express **12** 074001 (2019)

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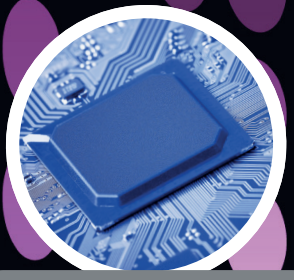

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